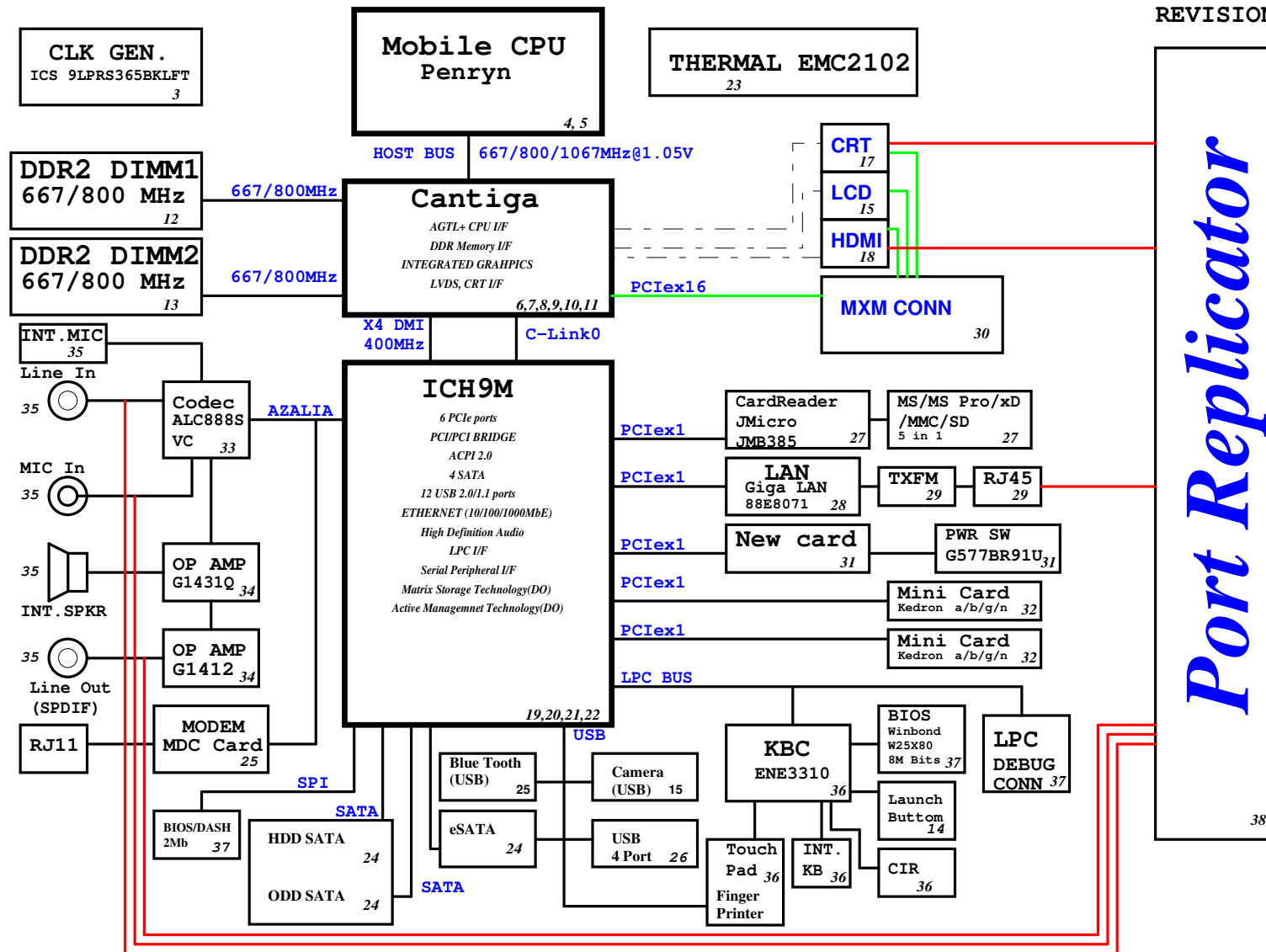


Eiger Block Diagram

Project code: 91.4Z501.001
PCB P/N : 48.4Z501.001
REVISION : 07246- -1



PCB STACKUP

TOP	_____
VCC	_____
S	_____
S	_____
GND	_____
BOTTOM	_____

SYSTEM DC/DC	
TPS51125 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
SYSTEM DC/DC	
TPS51124 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
RT9026 44	
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3
RT9018A 44	
1D8V_S3	1D5V_S0
G9131 44	
3D3V_S0	2D5V_S0
GFXXCORE DC/DC	
ISL6263 46	
INPUTS	OUTPUTS
DCBATOUT	VGFXXCORE 0.7~1.25V
CPU DC/DC	
ISL6266A 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S 0.35~1.5V
CHARGER	
BQ24745 47	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

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Title			
BLOCK DIAGRAM			
Size Custom	Document Number		Rev
	Eiger		-1
Date: Tuesday, April 01, 2008	Sheet 1	of	50

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

PCIE Routing

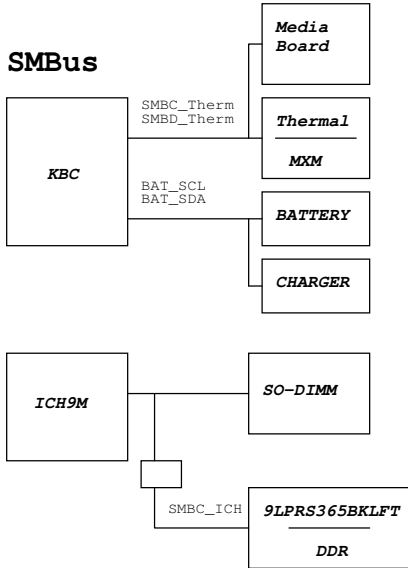
LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN/TV
LANE4	JMB385 Card Reader
LANE5	NewCard
LANE6	NC

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USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	USB5 (DOCK)
4	USB3
5	Bluetooth
6	FP
7	MINIC1
8	WEBCAM
9	NEW1
10	MINIC2
11	NC

SMBus



ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRS1PVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes x4 mode[MCH -> ICH]: (3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]: (3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCie are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
- Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

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Title		Reference		Rev
Size A3	Document Number	Eiger		-1
Date: Tuesday, April 01, 2008	Sheet 2	of 50		

6 H_A#(35..3) <<< H_A#(35..3)

H_DINV#(3..0) <<< H_DINV#(3..0) 6
H_DSTBN#(3..0) <<< H_DSTBN#(3..0) 6
H_DSTBP#(3..0) <<< H_DSTBP#(3..0) 6
H_D#(63..0) <<< H_D#(63..0) 6

Side Band
Non GTL

6 H_ADSTB#0 <<< H_REQ#(4..0)
19 H_A20M# <<< A20M#
19 H_FERR# <<< FERR#
19 H_IGNNE# <<< IGNNE#
19 H_STPCLK# <<< STPCLK#
19 H_INTR# <<< INTR#
19 H_NMI# <<< NMI#
19 H_SM# <<< SM#

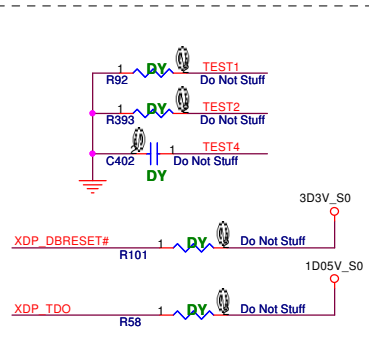
Do Not StuffP19 RSVD#M4
Do Not StuffP18 RSVD#M5
Do Not StuffP17 RSVD#M6
Do Not StuffP16 RSVD#M7
Do Not StuffP27 RSVD#M8
Do Not StuffP31 RSVD#M9
Do Not StuffP24 RSVD#M10
Do Not StuffP28 RSVD#M11
Do Not StuffP26 RSVD#M12
Do Not StuffP22 RSVD#M13
Do Not StuffP32 RSVD#M14

BGA479-SKT-8-GP-U2
62.10053.401
62.10079.001

XDP TMS R321 1 54D9R2F-L1-GP
XDP TDI R320 1 54D9R2F-L1-GP
XDP BPM#5 R324 1 54D9R2F-L1-GP
H_CPURST# R106 1 Do Not Stuff
XDP TRK R323 1 54D9R2F-L1-GP
XDP TRST# R322 1 54D9R2F-L1-GP

All place within 2" to CPU

Follow Demo Circuit

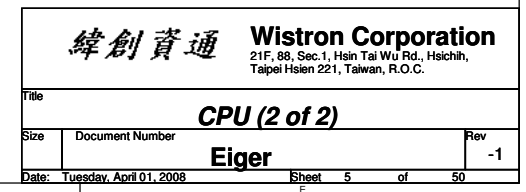


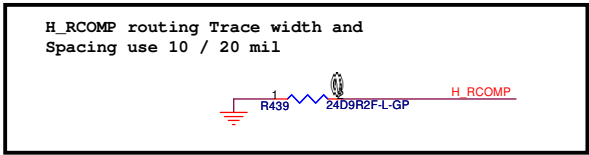
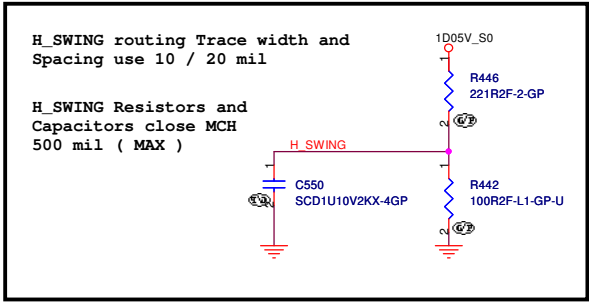
Net "TEST4" as short as possible,
make sure "TEST4" routing is
reference to GND and away other
noisy signals

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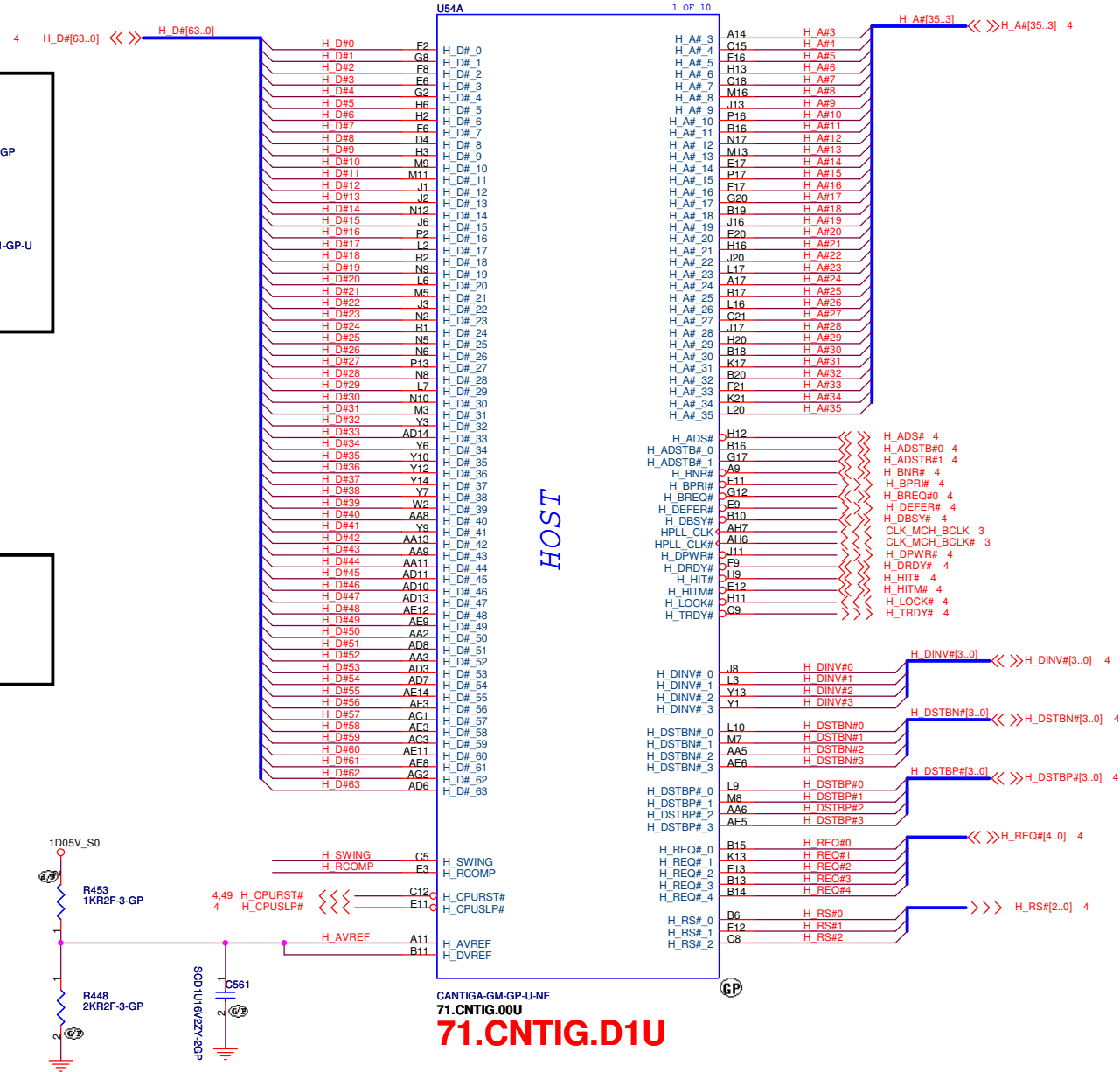
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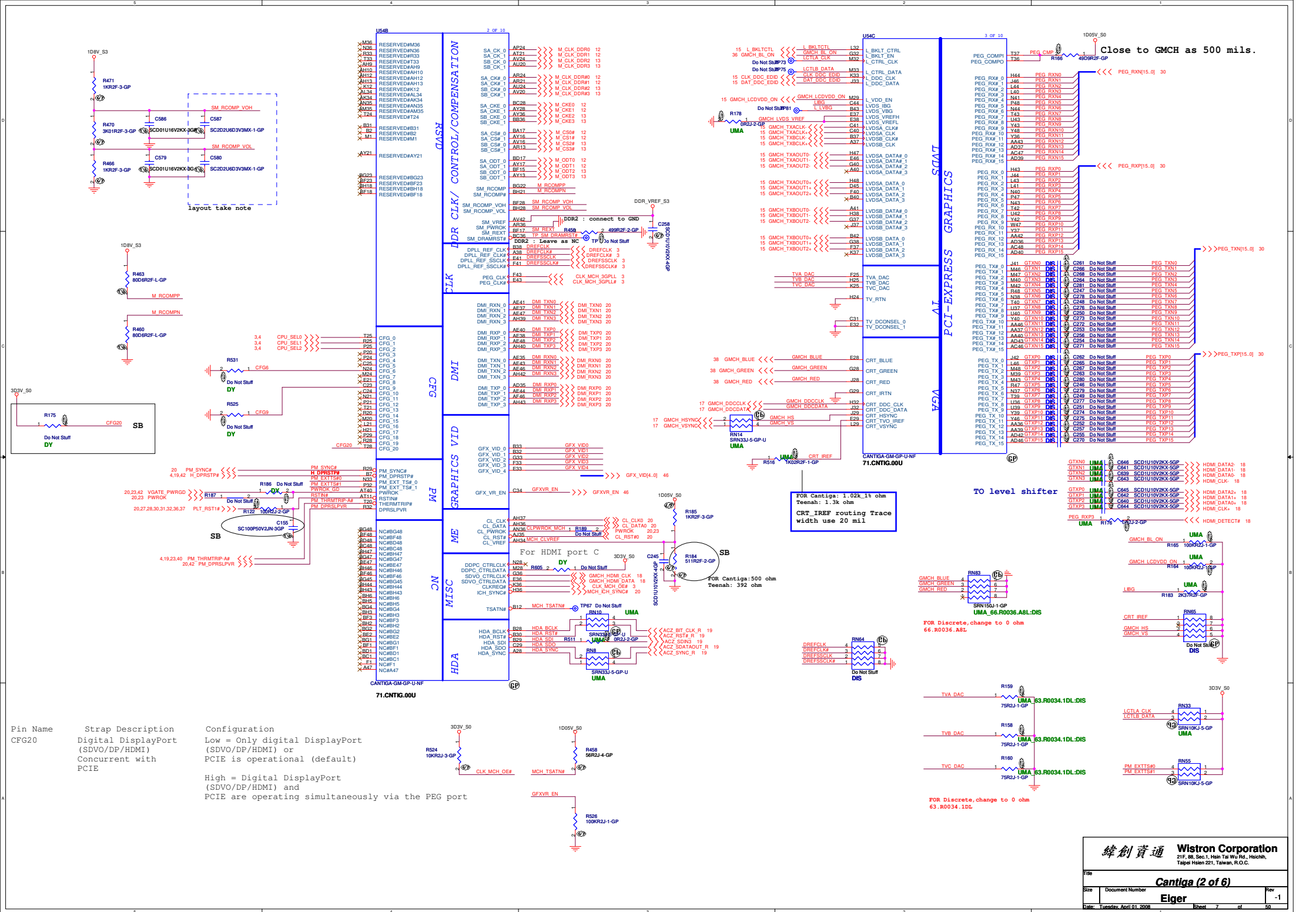
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Size Document Number
Date: Tuesday, April 01, 2008 Sheet 4 of 50
Eiger
Rev -1

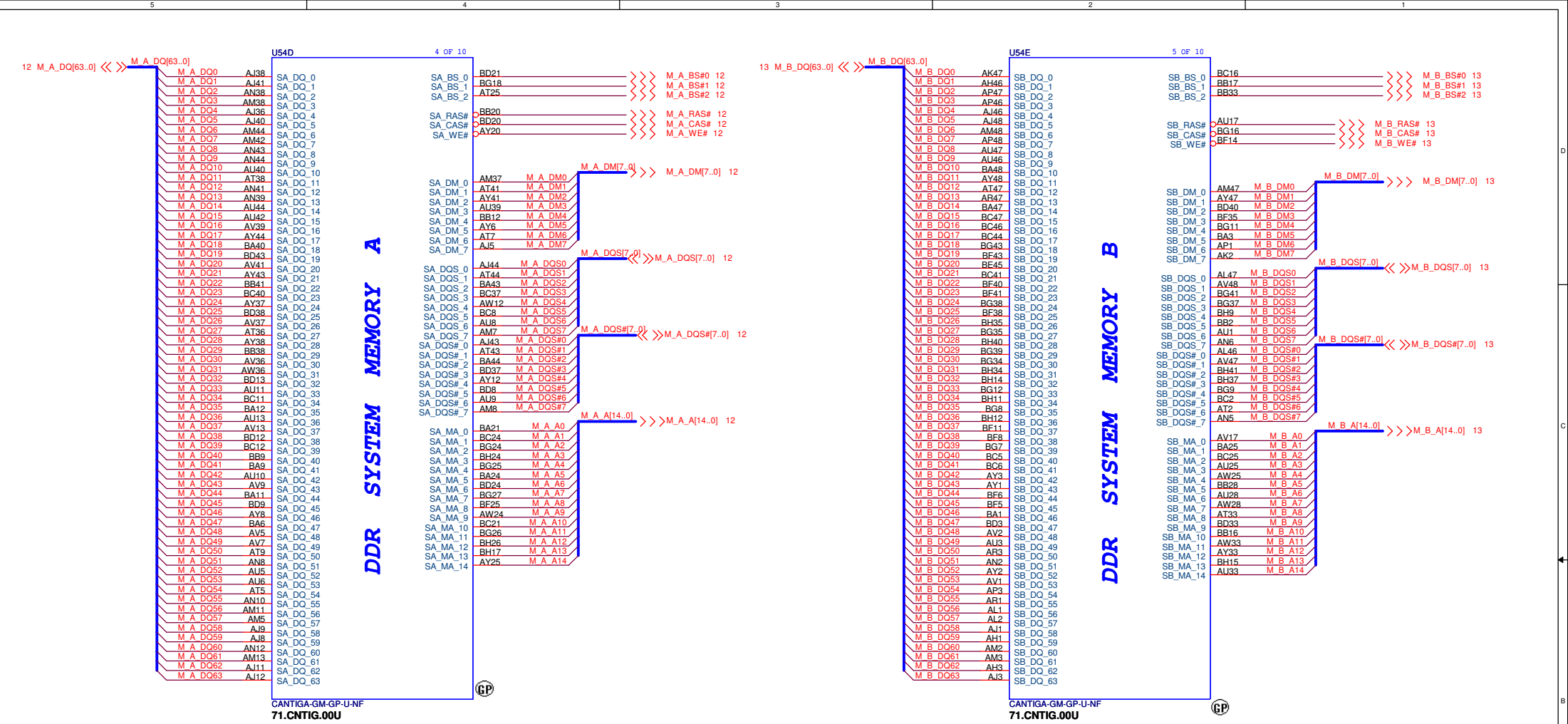


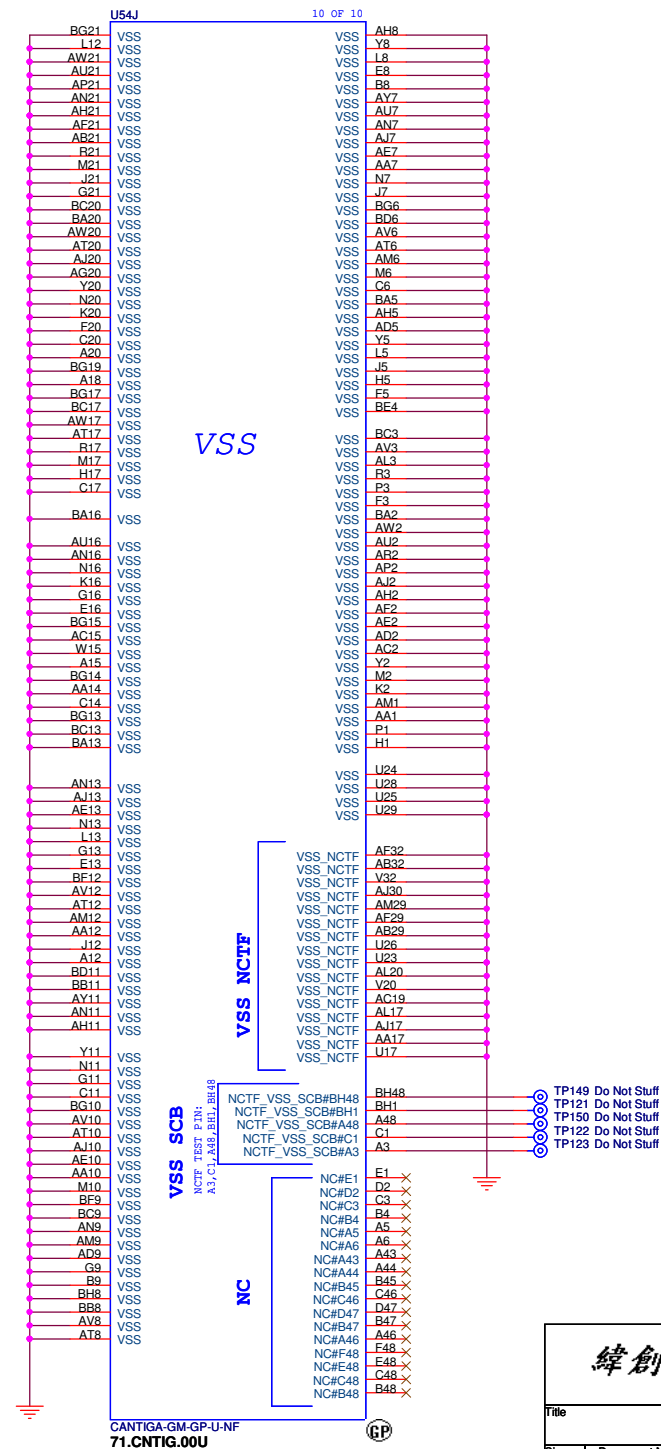
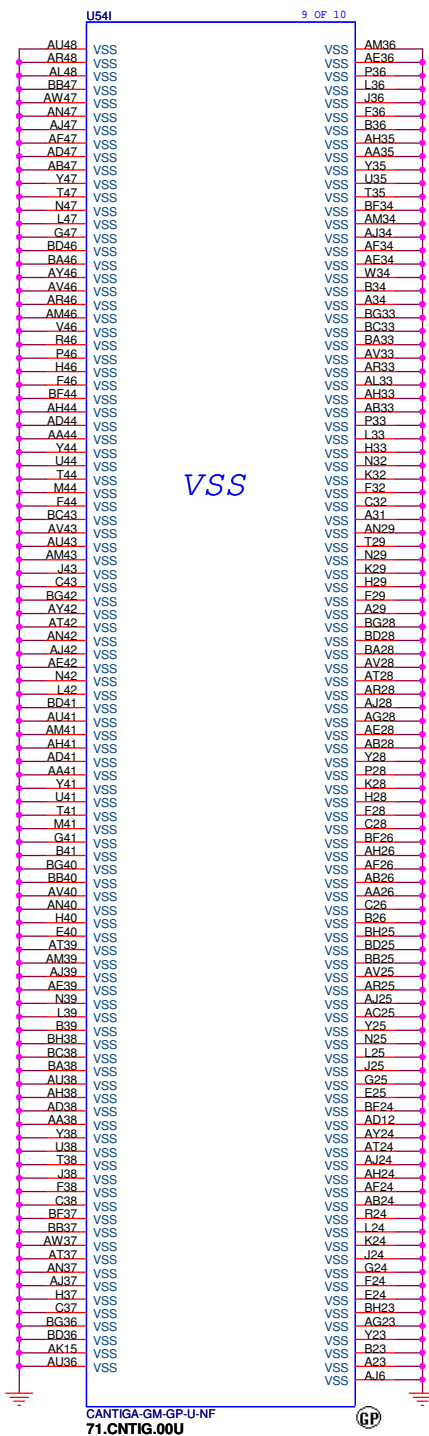


Place them near to the chip (< 0.5"

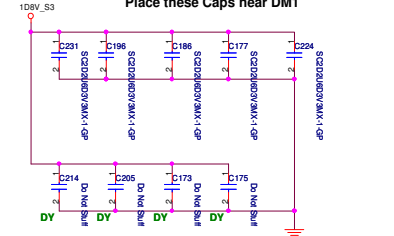








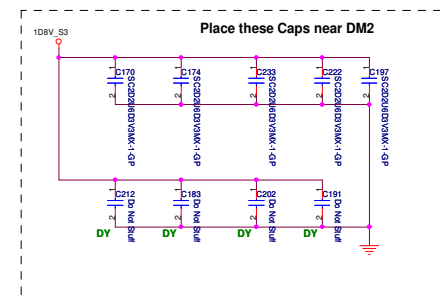
Put decap near power(0.9V) and pull-up resistor

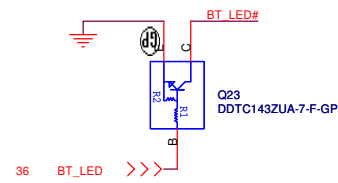
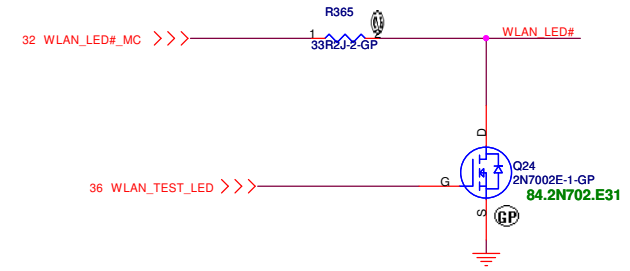
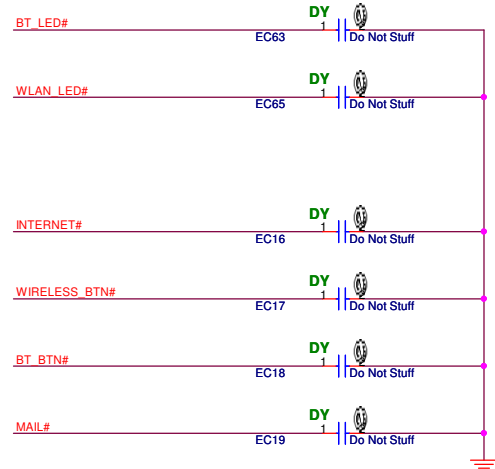
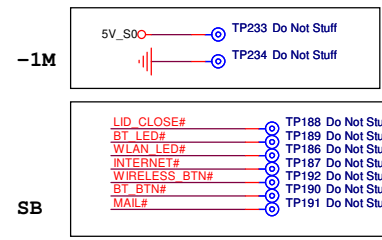
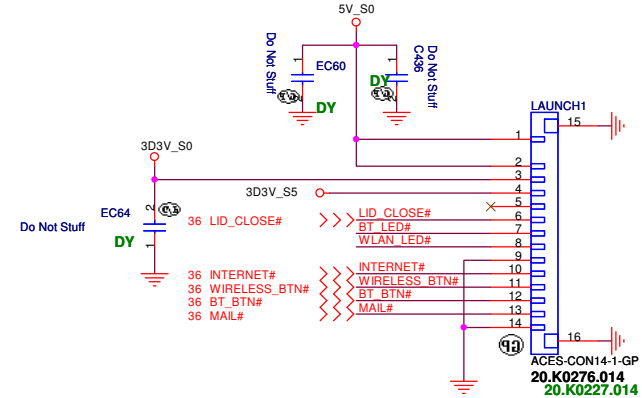
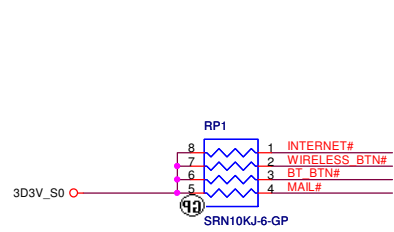


Put decap near power(0.9V) and pull-up resistor

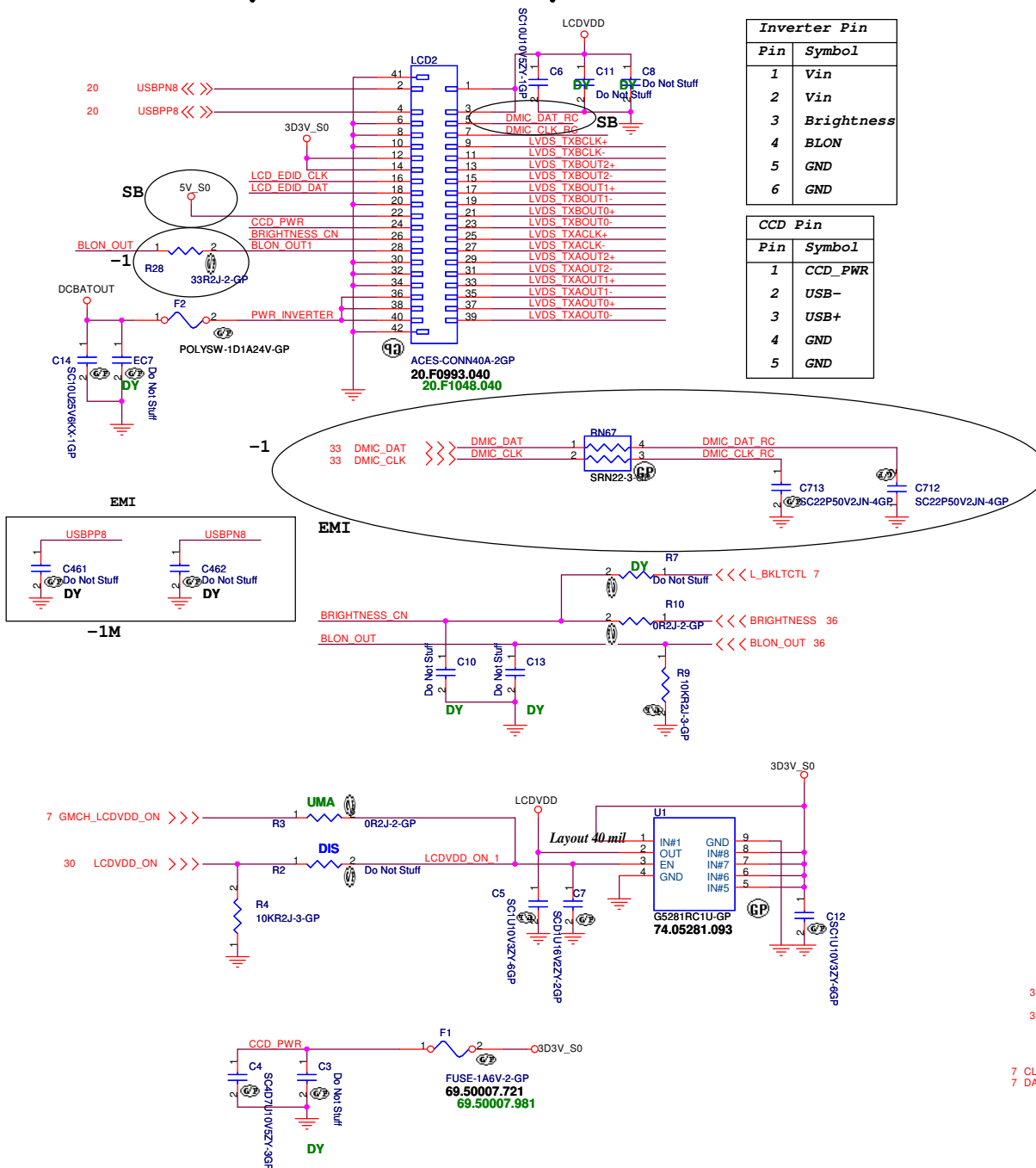


*Put decap near power(0.9V)
and pull-up resistor*



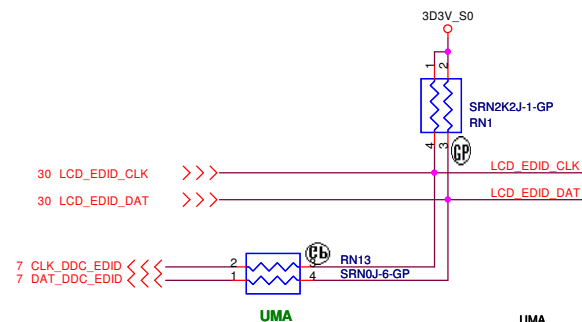
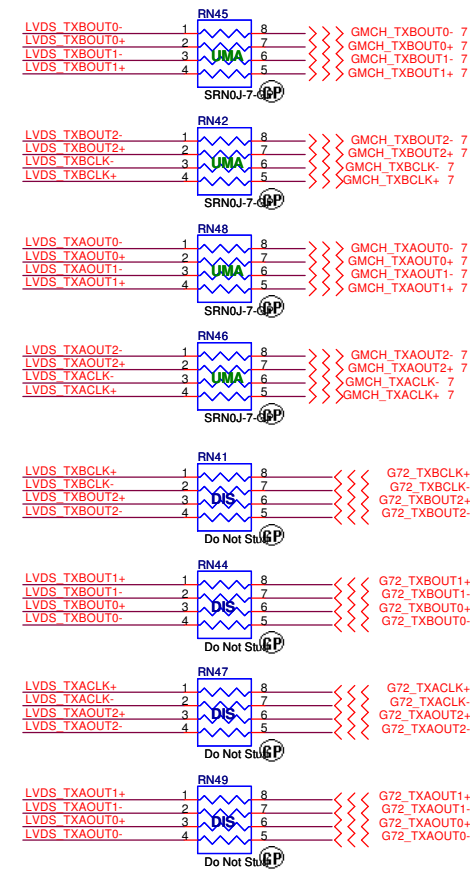


LCD/INVERTER/CCD CONN



<i>Inverter Pin</i>	
<i>Pin</i>	<i>Symbol</i>
1	<i>Vin</i>
2	<i>Vin</i>
3	<i>Brightness</i>
4	<i>BLON</i>
5	<i>GND</i>
6	<i>GND</i>

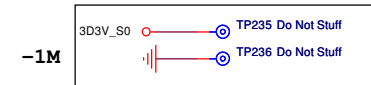
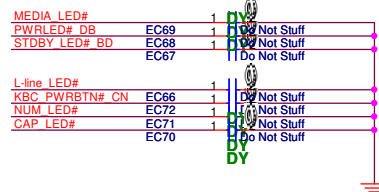
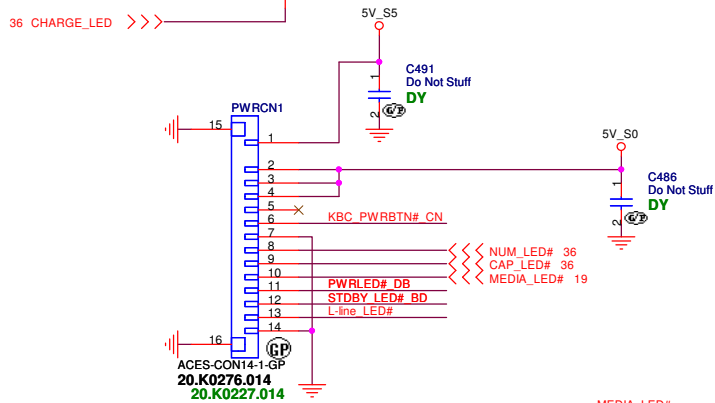
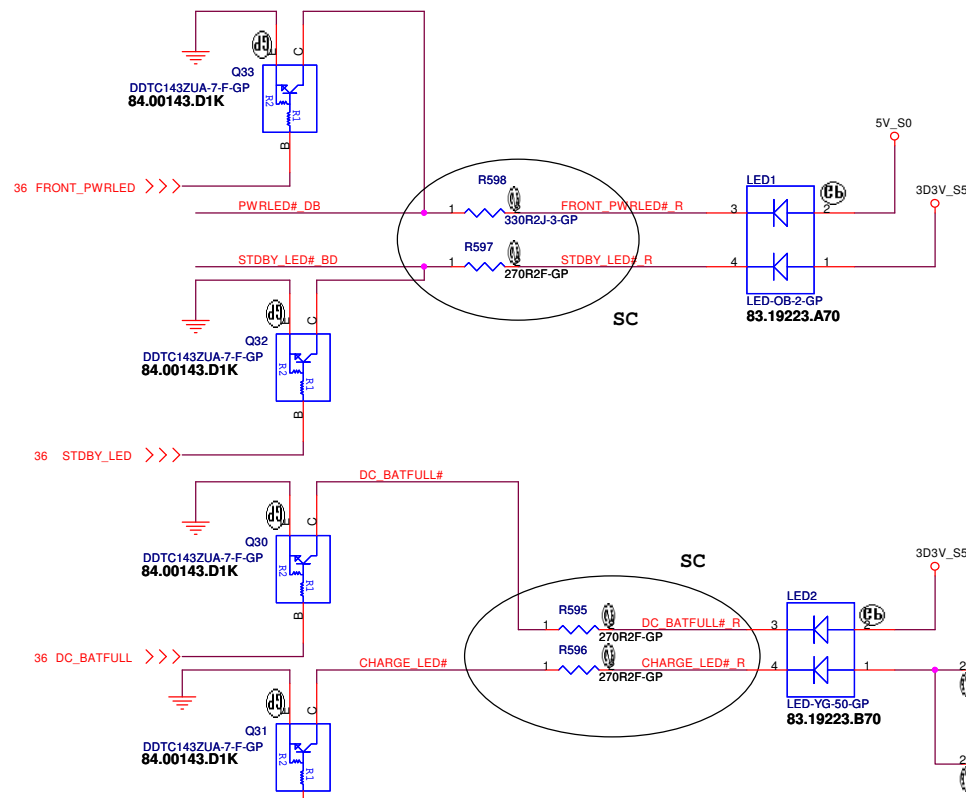
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



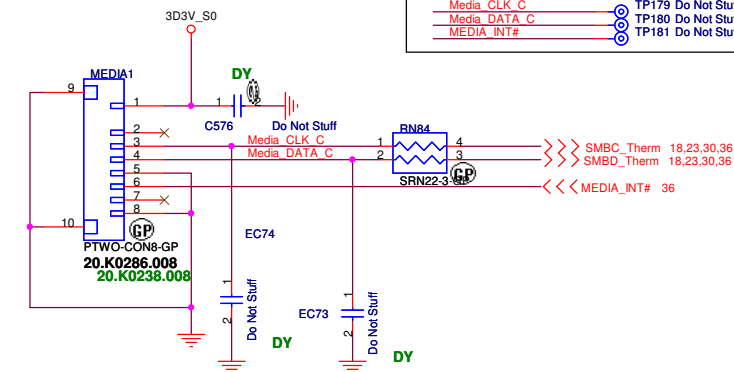
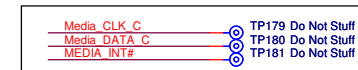
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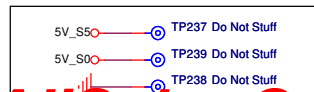
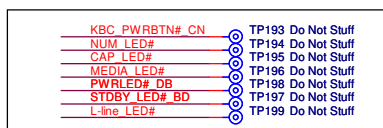
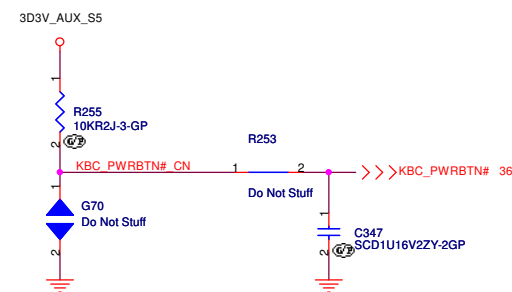
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LCD CONN			
Size	Document Number		Rev
	Eiger		-1
Date:	Tuesday, April 01, 2008	Sheet 15 of	50



SB



MEDIA BOARD



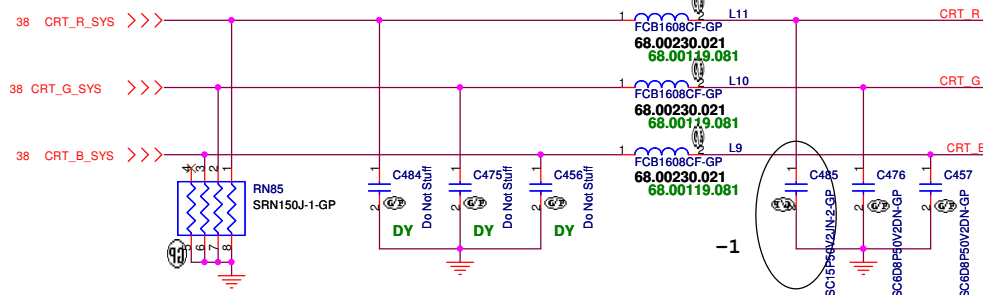
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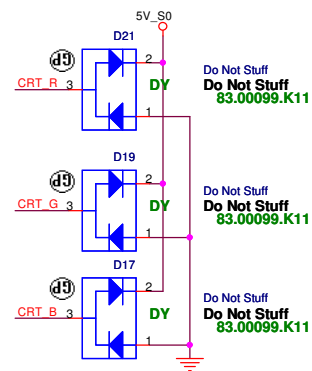
Title		Power & Media Board	
Size	Document Number	Eiger	
Date: Tuesday, April 01, 2008	Sheet 16 of 50	Rev -1	

Layout Note:
Place these resistors
close to the CRT-out
connector

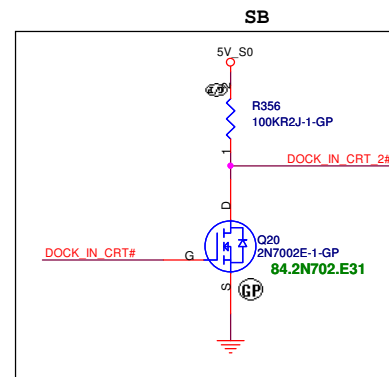
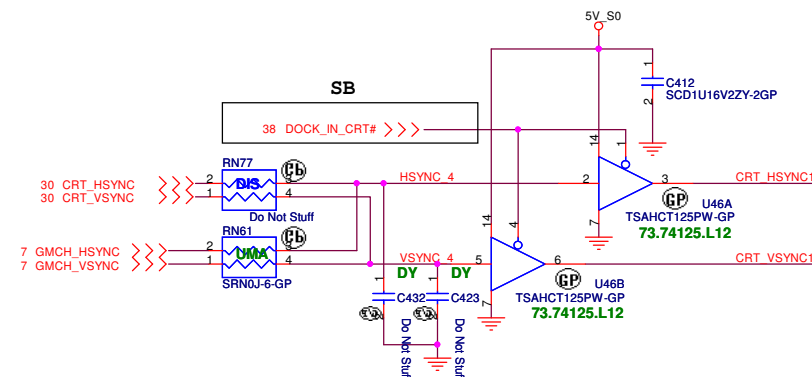
Ferrite bead impedance: 10 ohm@100MHz



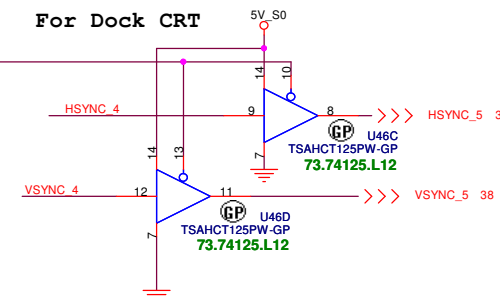
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



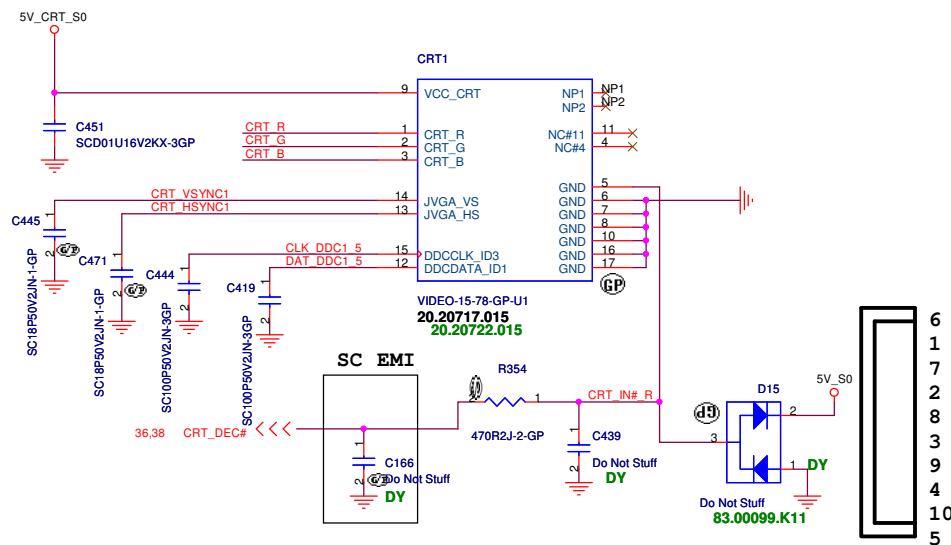
Hsync & Vsync level shift



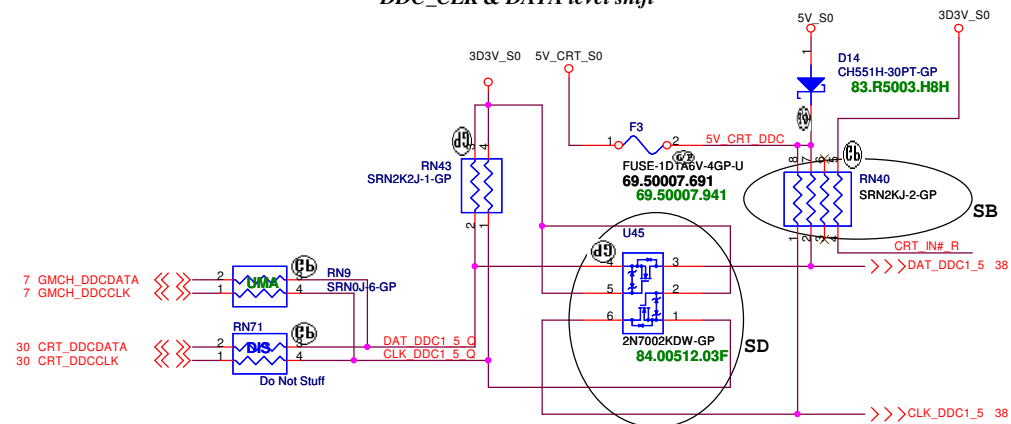
For Dock CRT



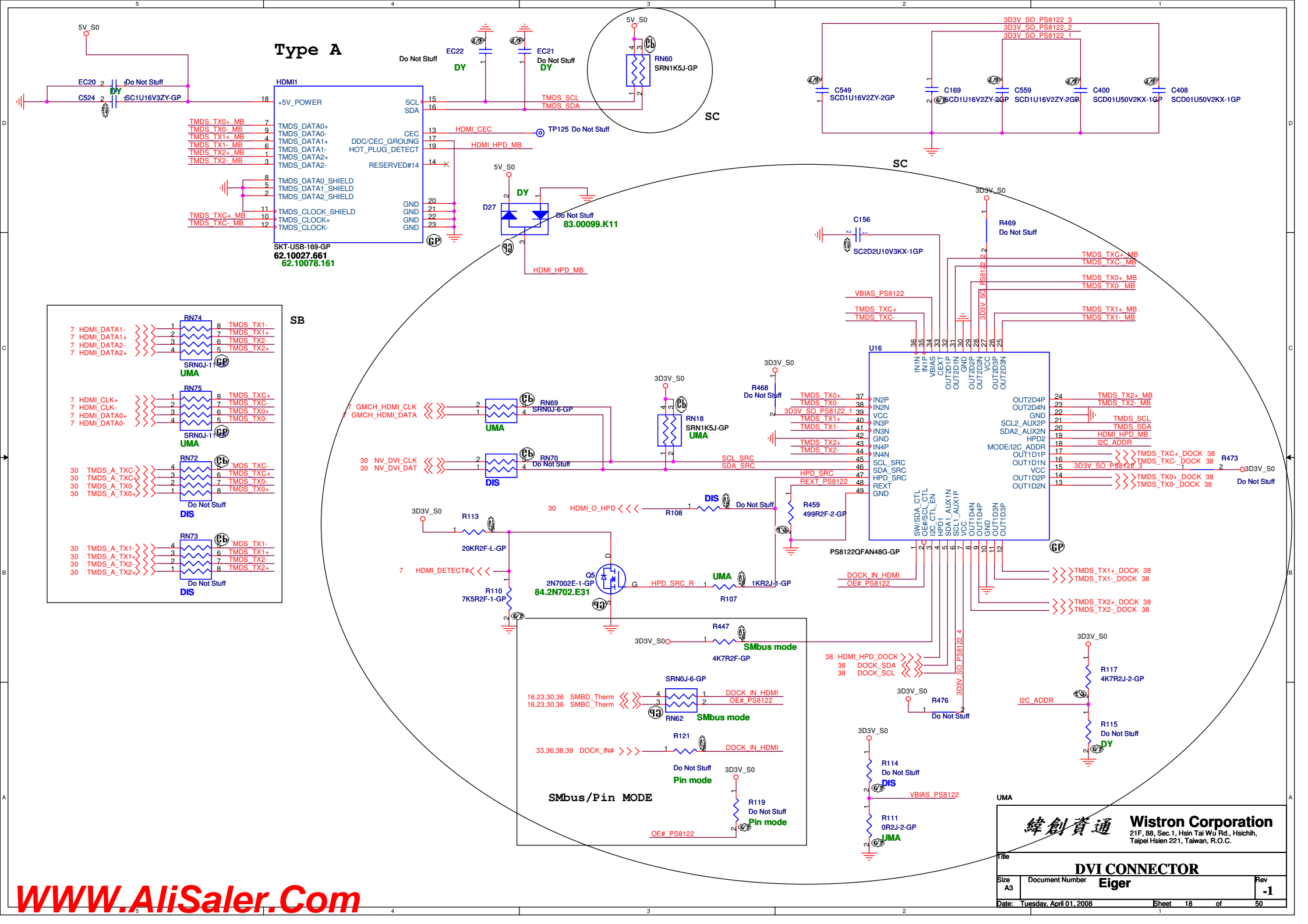
CRT I/F & CONNECTOR

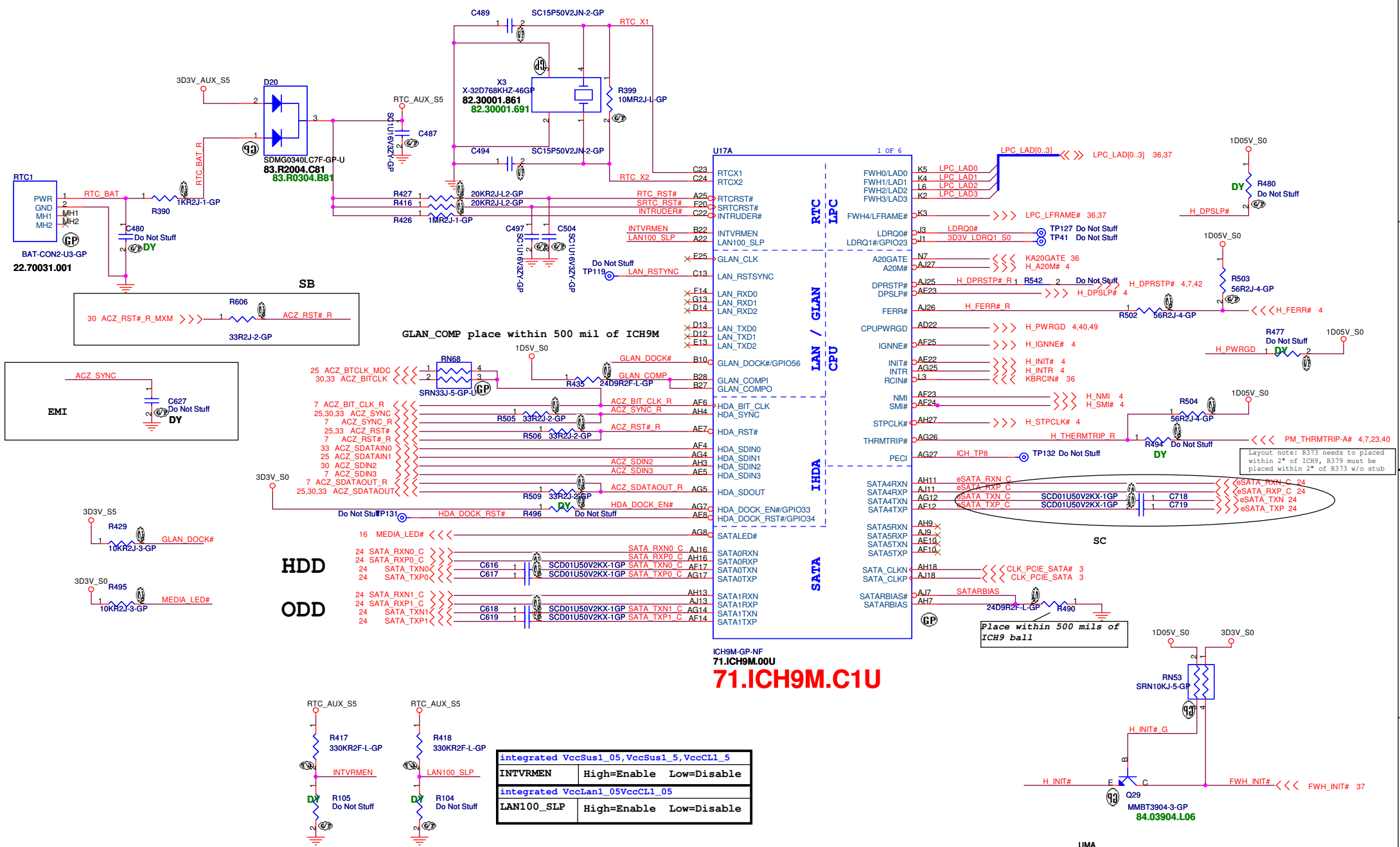


DDC_CLK & DATA level shift

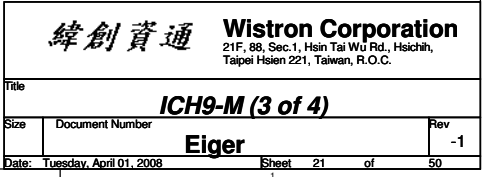


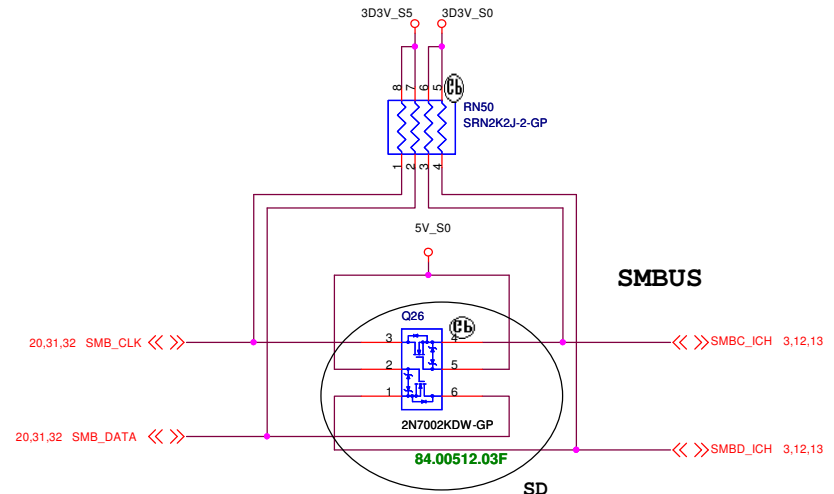
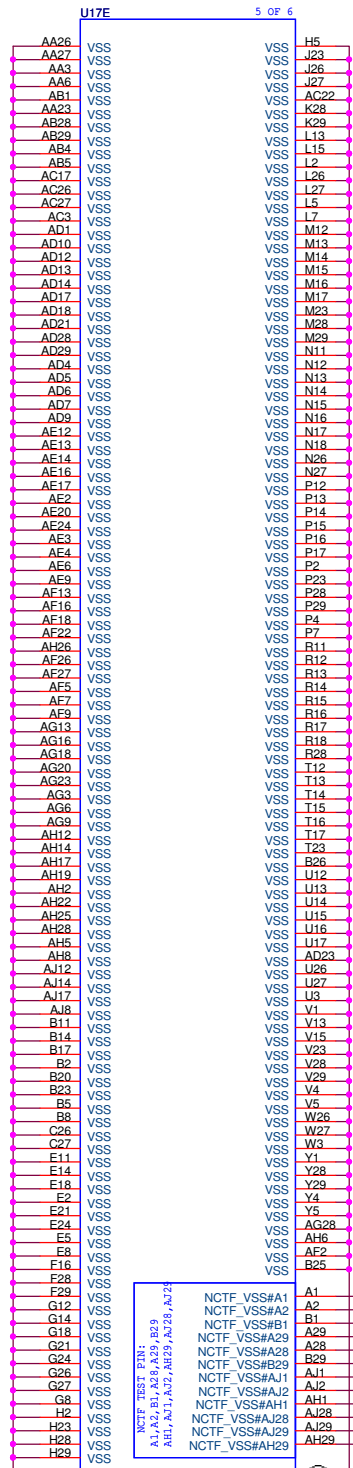
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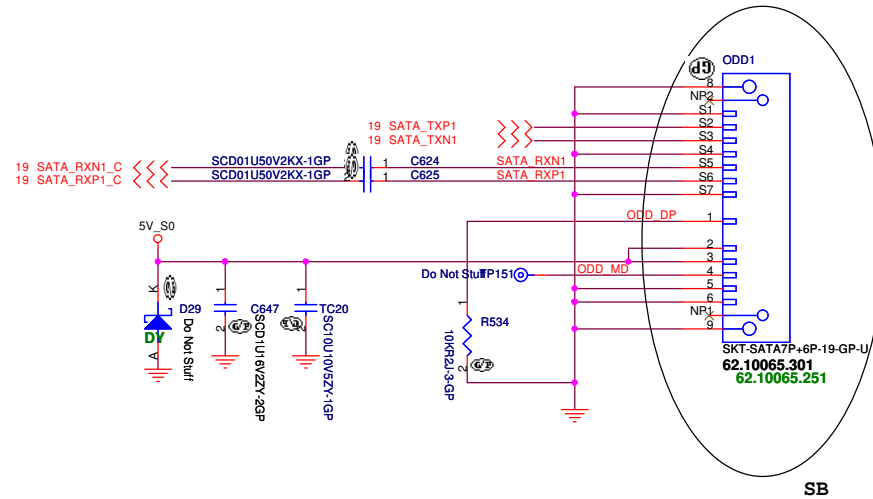
integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable



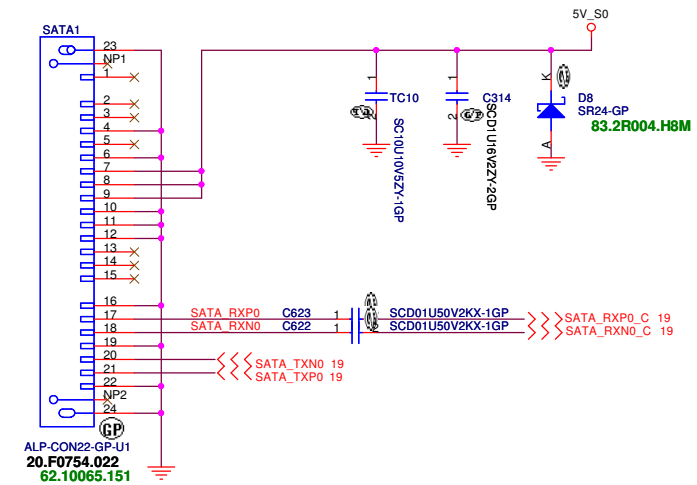




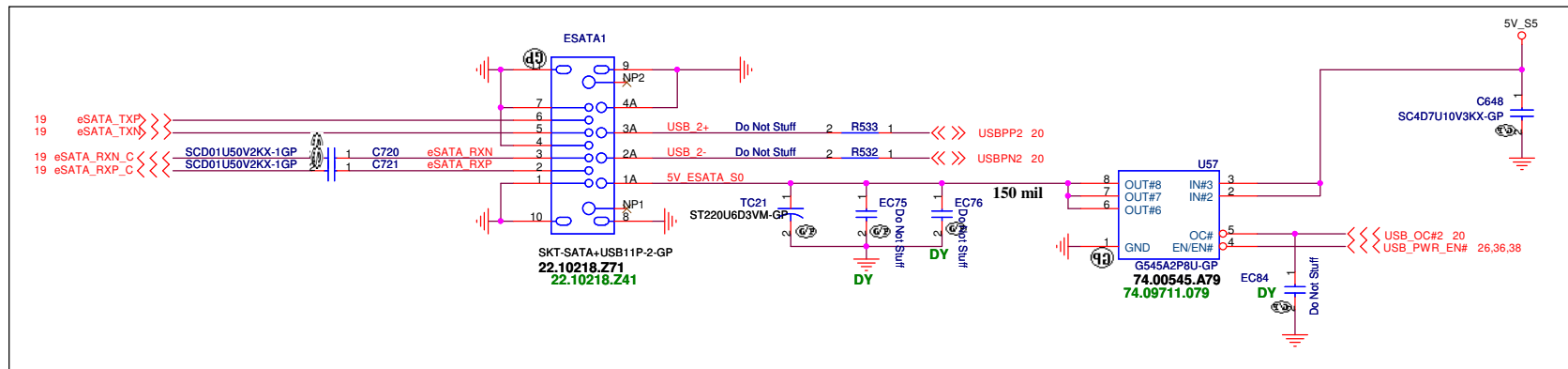
SATA ODD Connector



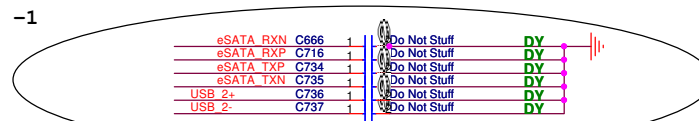
SATA Connector



SC



-1



EMI

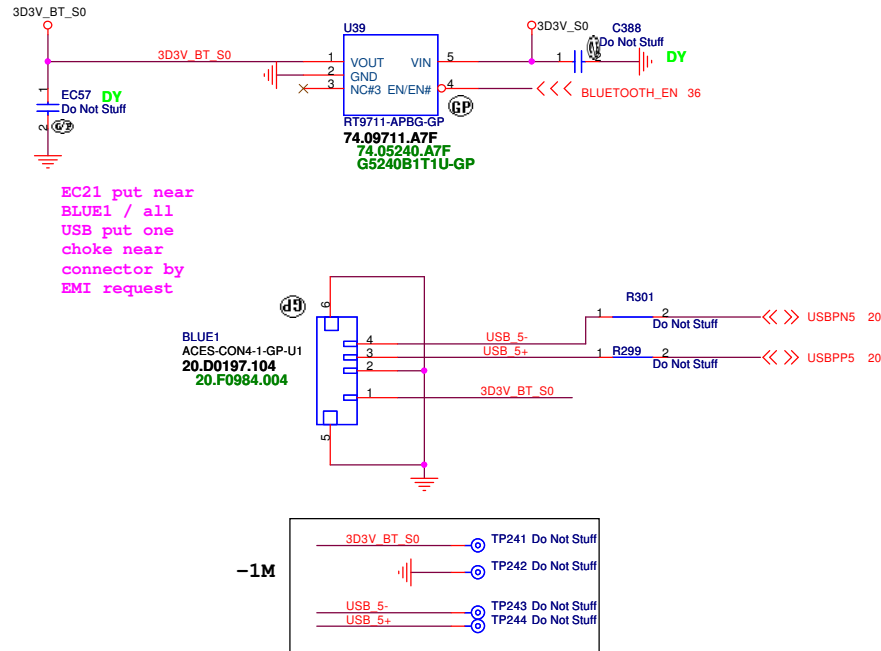
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Taipei Hsien 221, Taiwan, R.O.C.

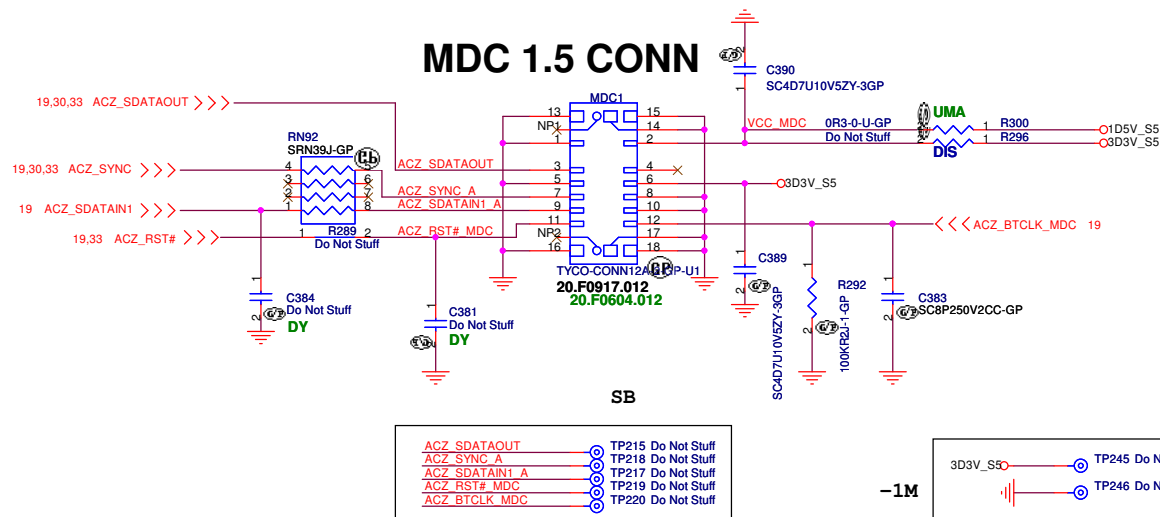
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Size	Document Number	Eiger	Rev
Date: Tuesday, April 01, 2008	Sheet 24	of 50	-1

BLUETOOTH MODULE

1.5A / High Active Voltage 2V



MDC 1.5 CONN



Finger printer

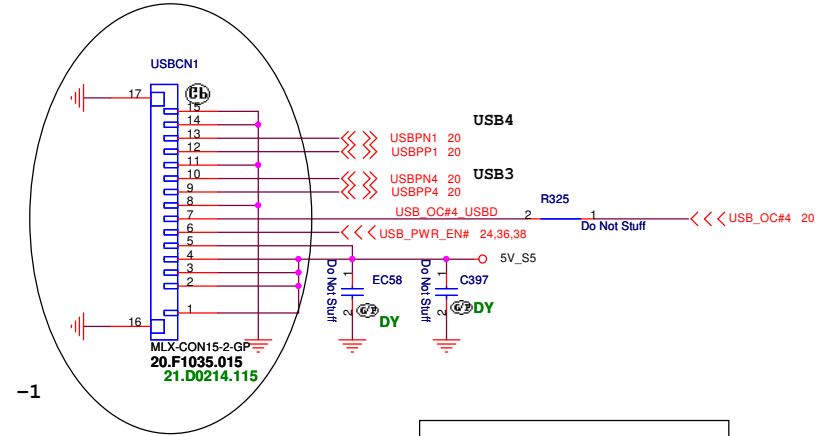
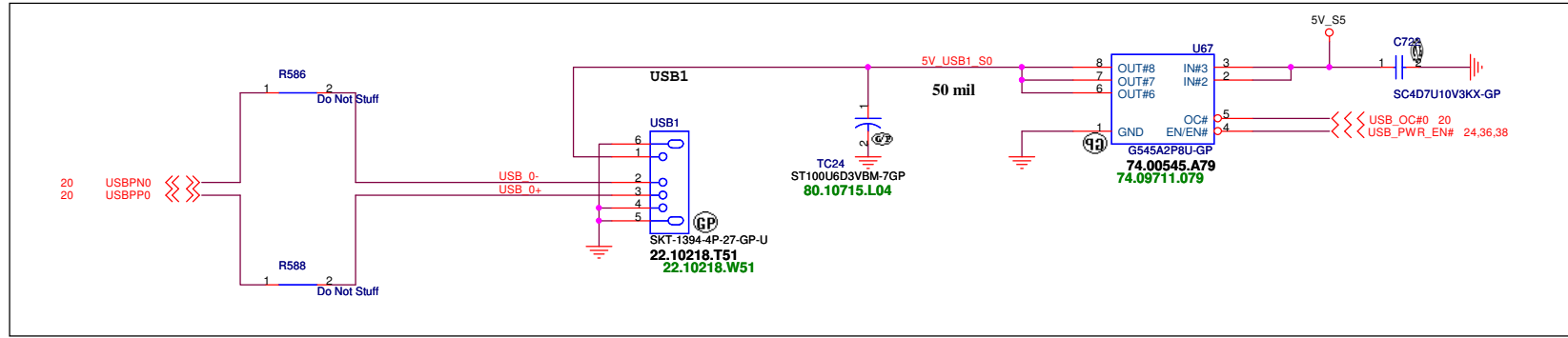
MOVE TO Page 36

UMA

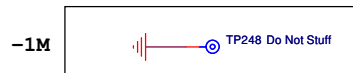
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

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Size		Document Number	
Date: Tuesday, April 01, 2008		Sheet 25 of 50	
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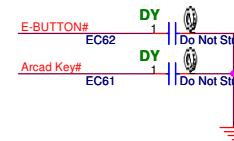
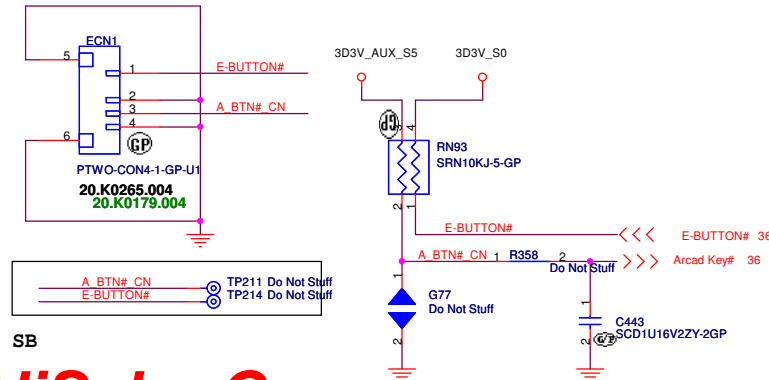
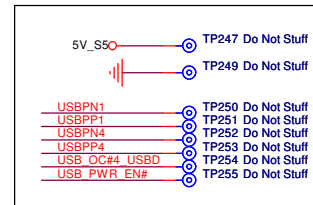
SC



ECN BOARD



-1M

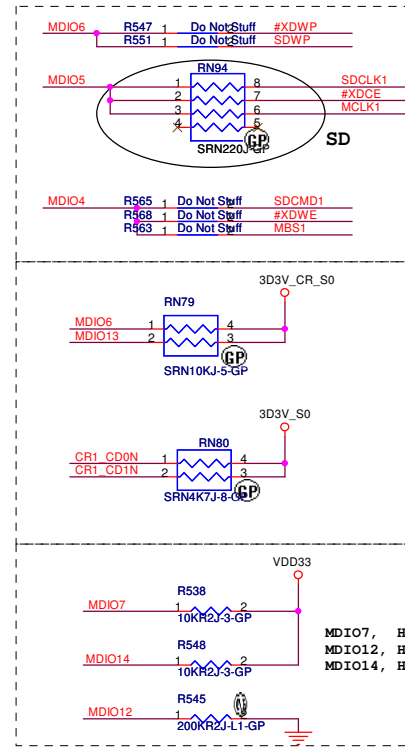


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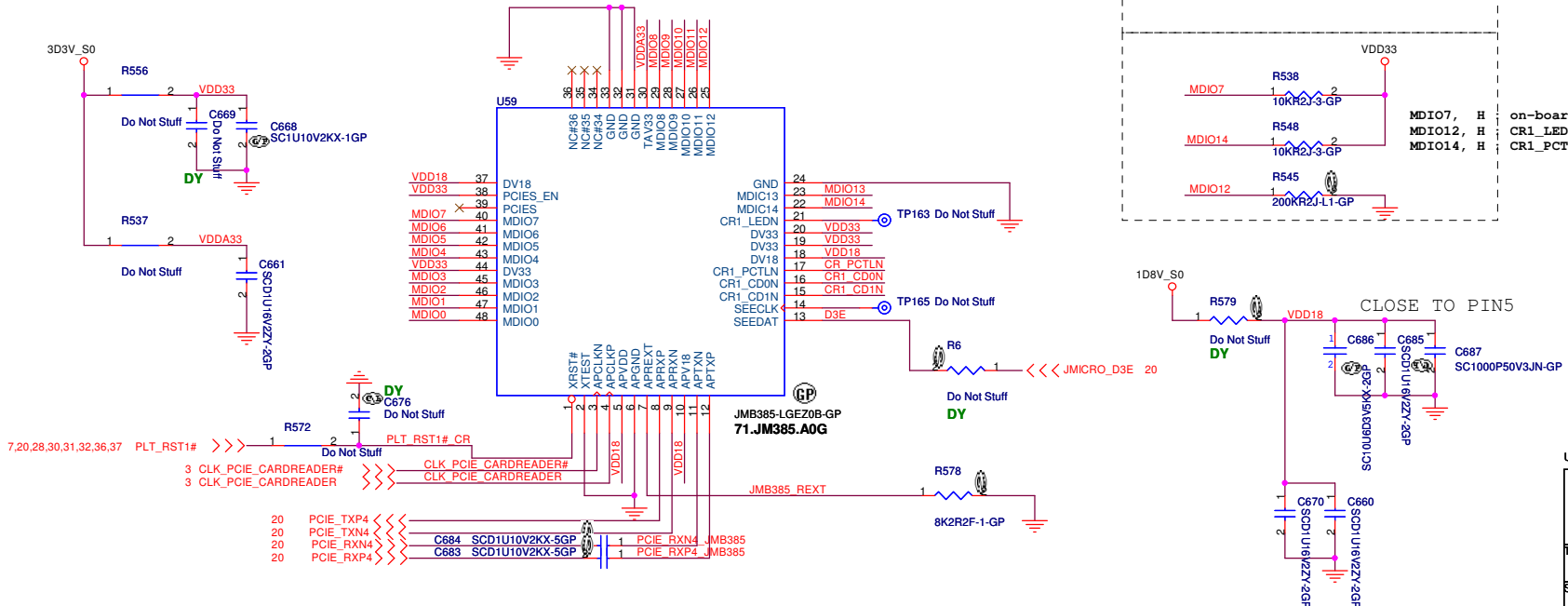
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Taipei Hsien 221, Taiwan, R.O.C.

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1.5A / High Active Voltage 2V



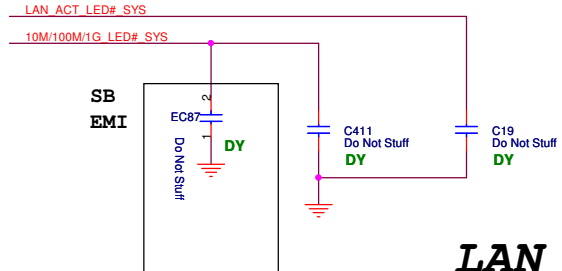
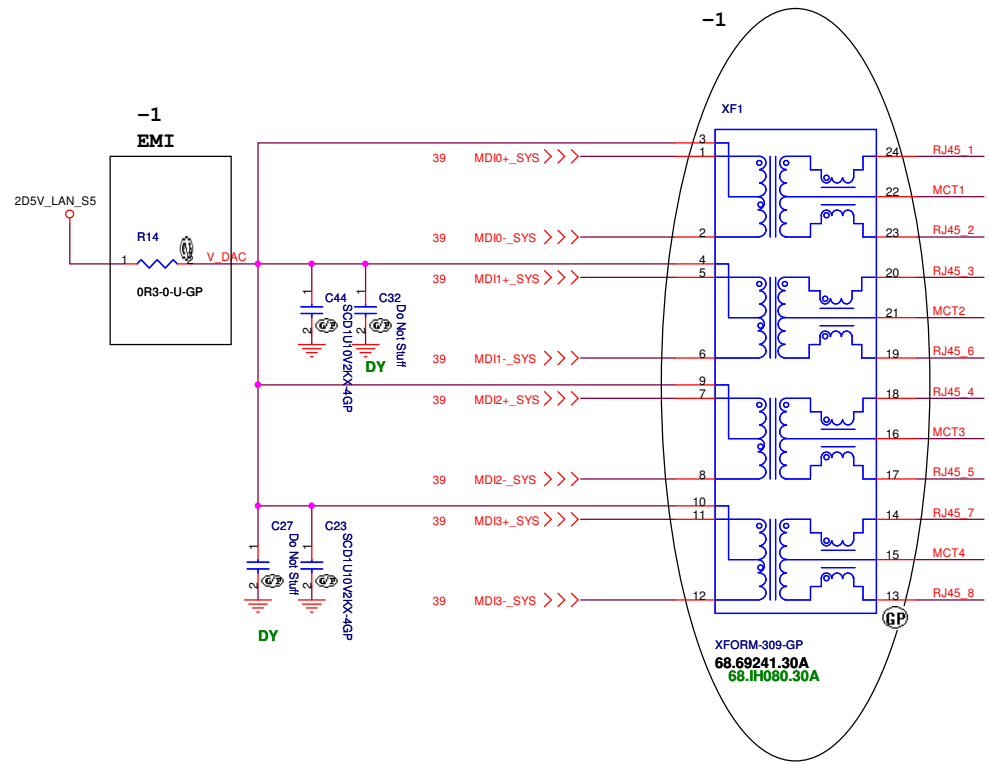
MADIO0	C555	1	2	Do Not Stuff	DY
MADIO1	C556	1	2	Do Not Stuff	DY
MADIO2	C597	1	2	Do Not Stuff	DY
MADIO3	C598	1	2	Do Not Stuff	DY
SDCMIO1	C602	1	2	Do Not Stuff	DY
SDCLK1	C603	1	2	Do Not Stuff	DY
CR1_C0DN	C714	1	2	Do Not Stuff	DY
SDWP	C715	1	2	Do Not Stuff	DY



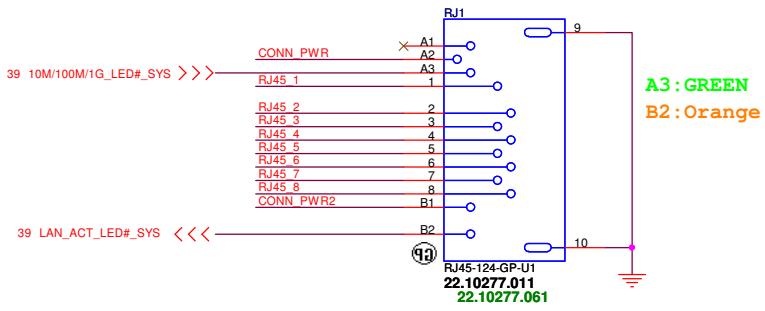
```
on-board, L : on Add-in card or Express card
CR1_LEDN high active, L : CR1_LEDN low active
CR1_PCTLN high active, L : CR1_PCTLN low active
```


LAN Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



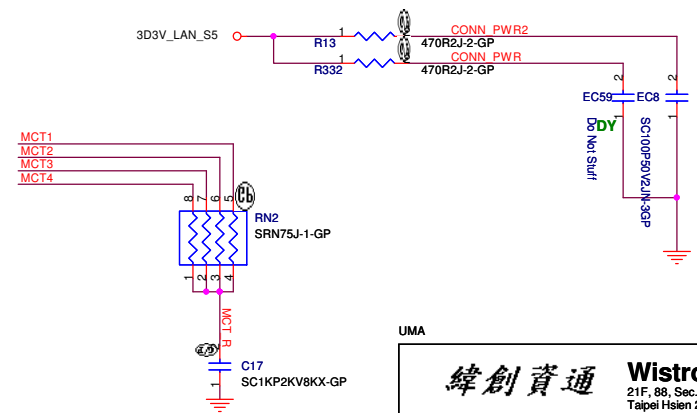
LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

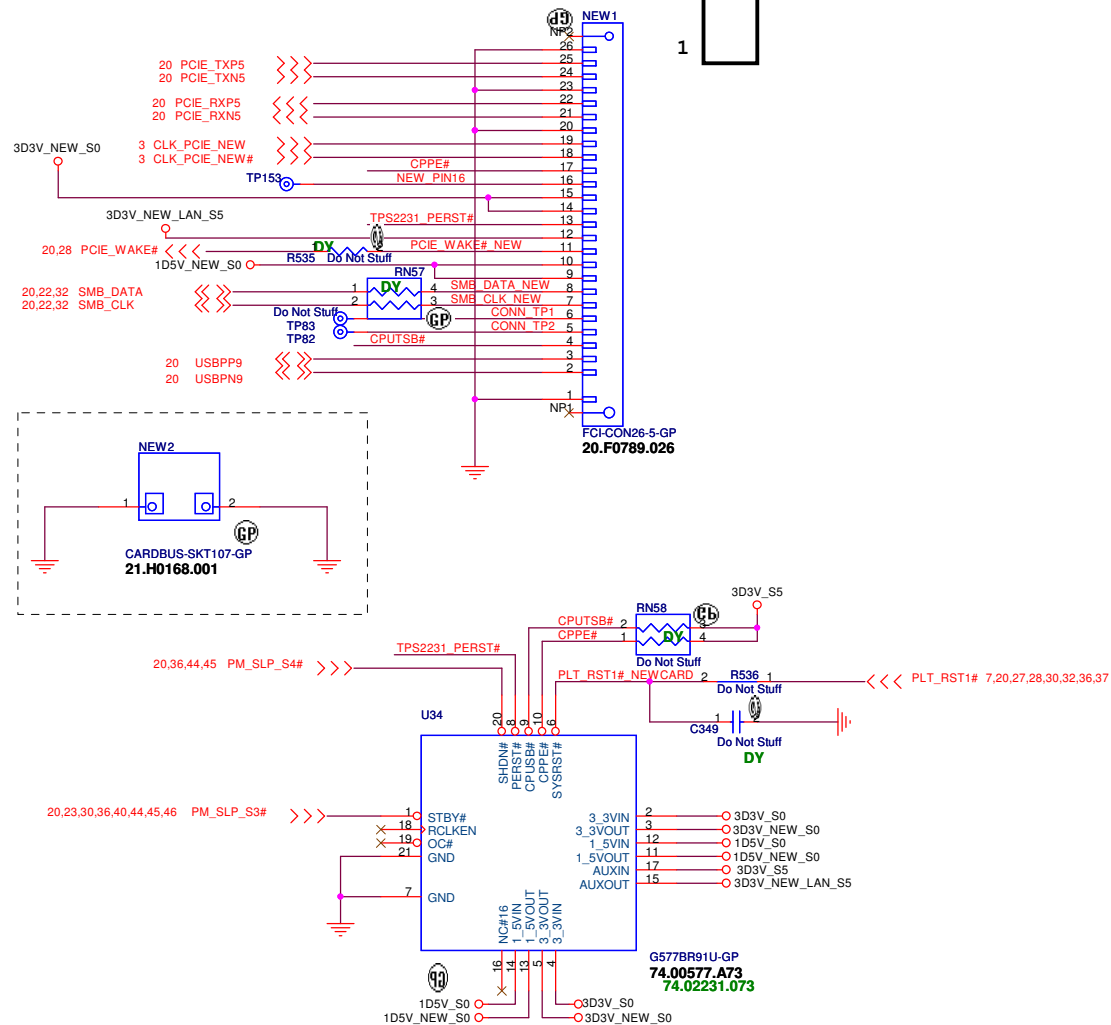
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



NEWCARD Connector

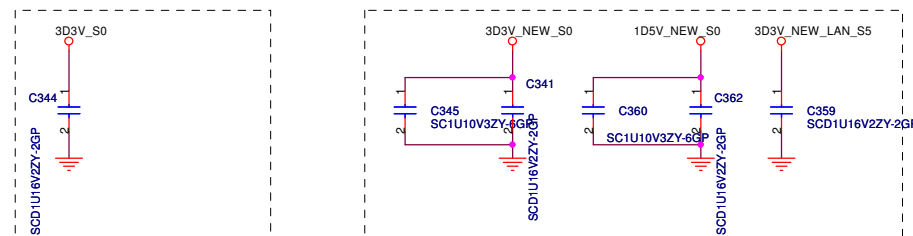
Reserve the symbol
for bottom side
connector

TOP VIEW



Place them Near to Chip

Place them Near to Connector

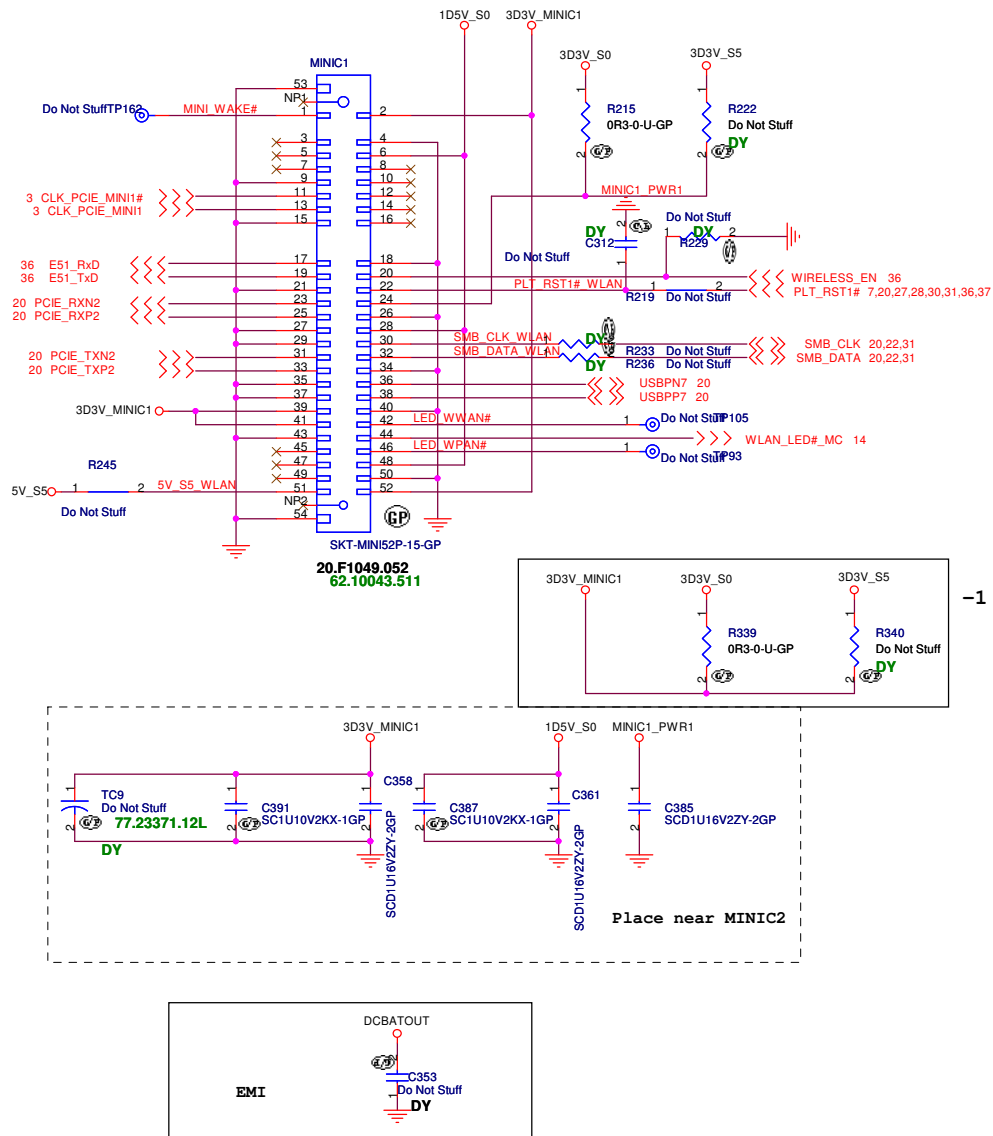


UMA

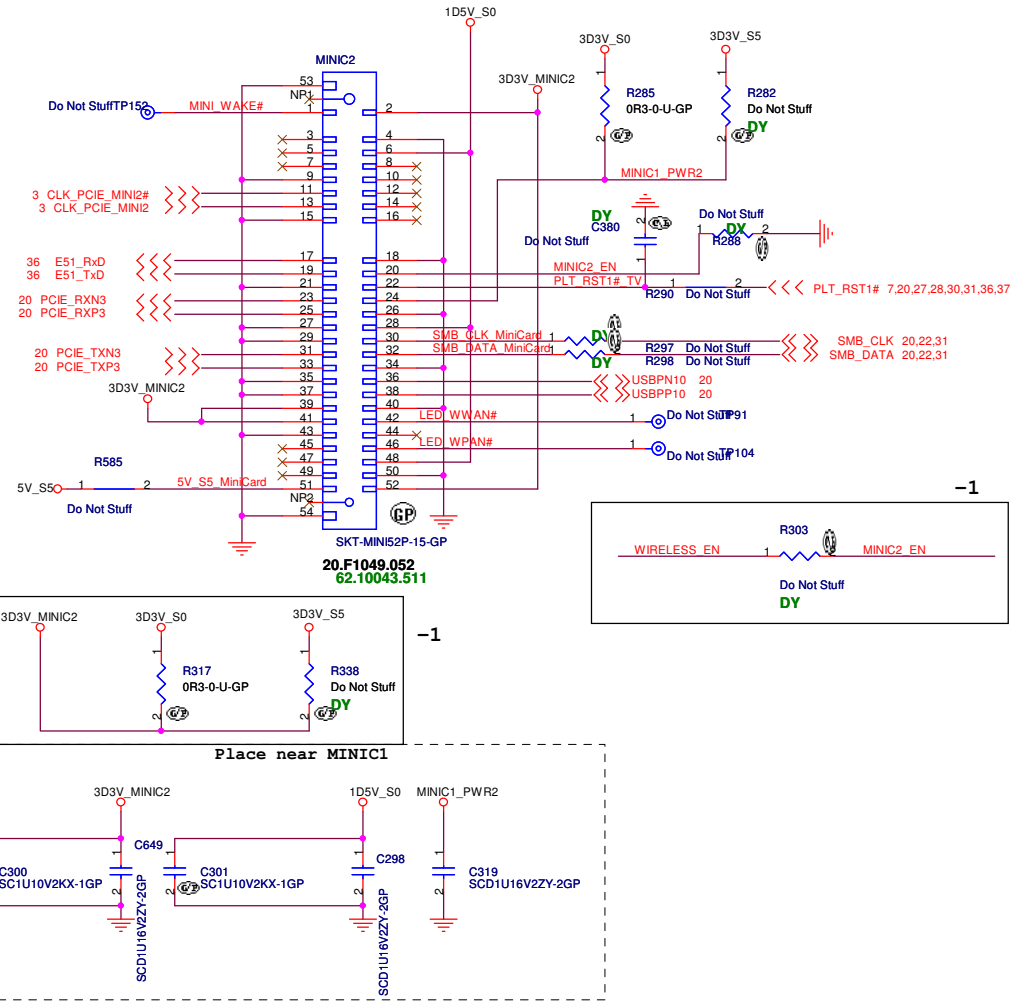
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Title		NEW CARD	
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Mini Card Connector(WLAN)

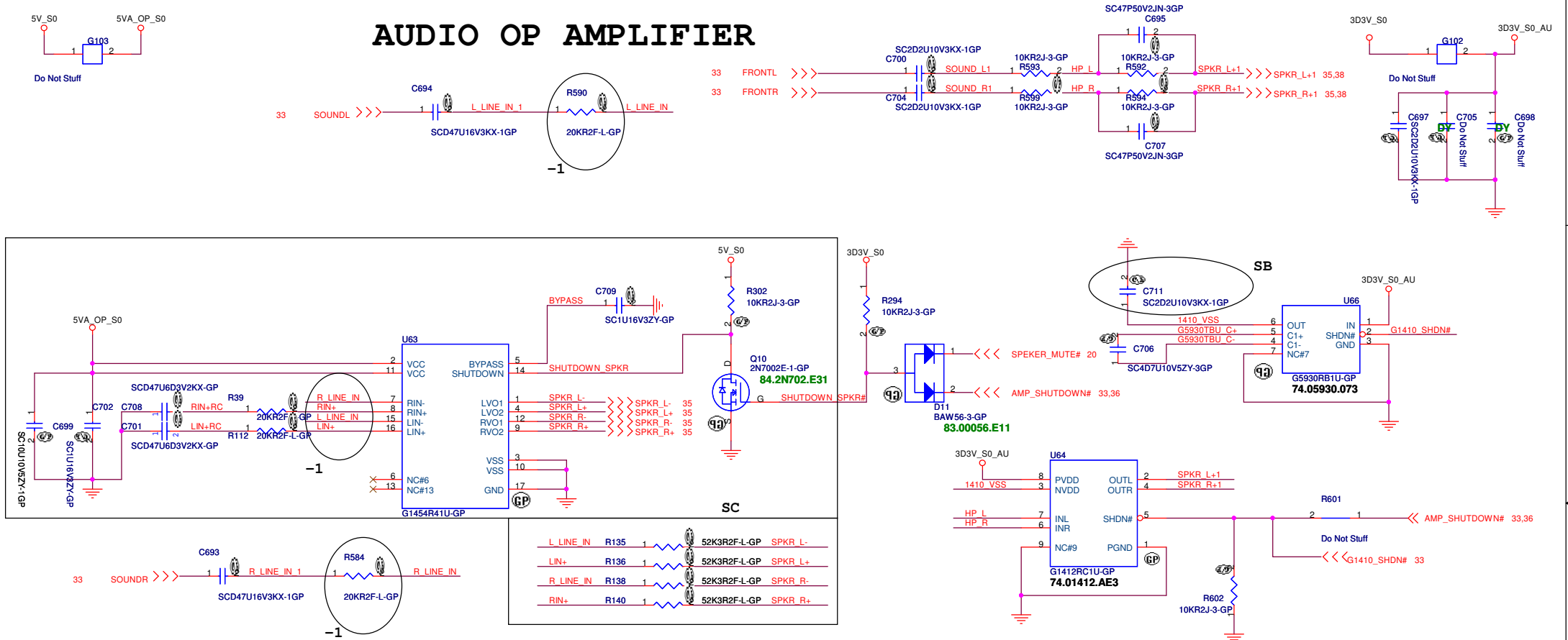


Mini Card Connector(TV)

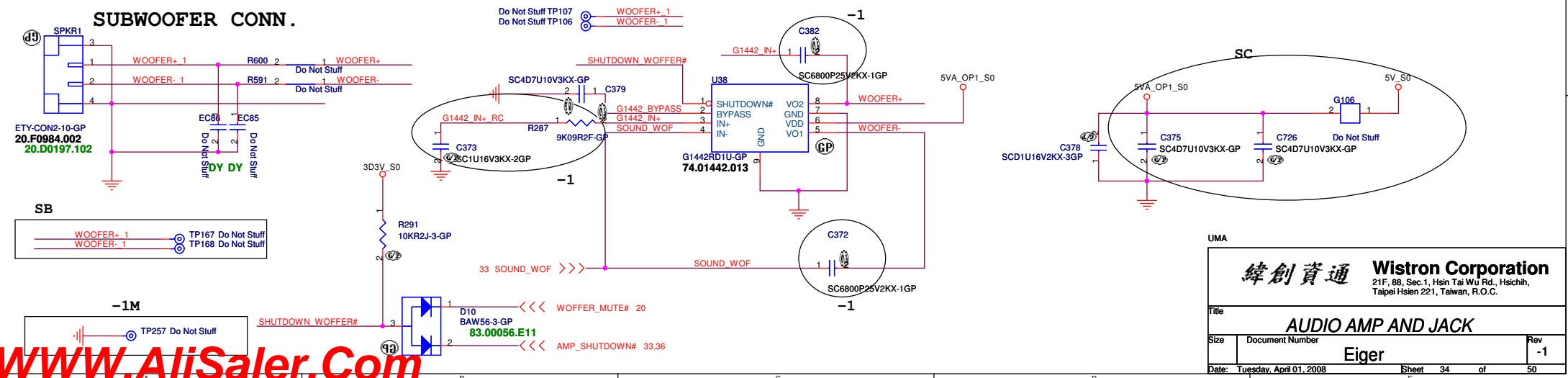


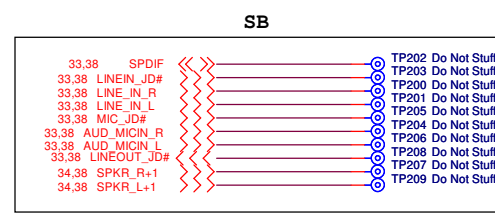
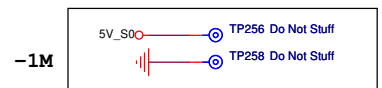
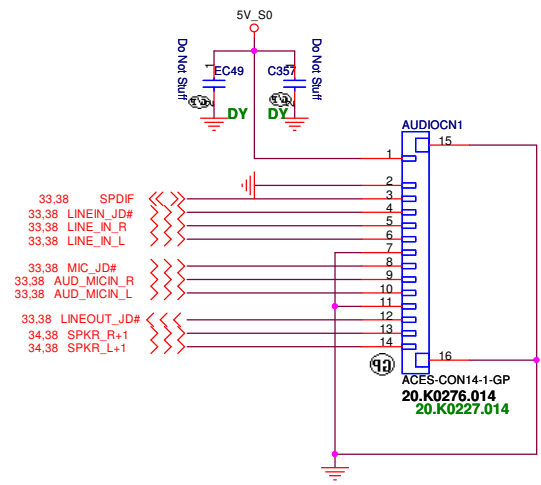


AUDIO OP AMPLIFIER

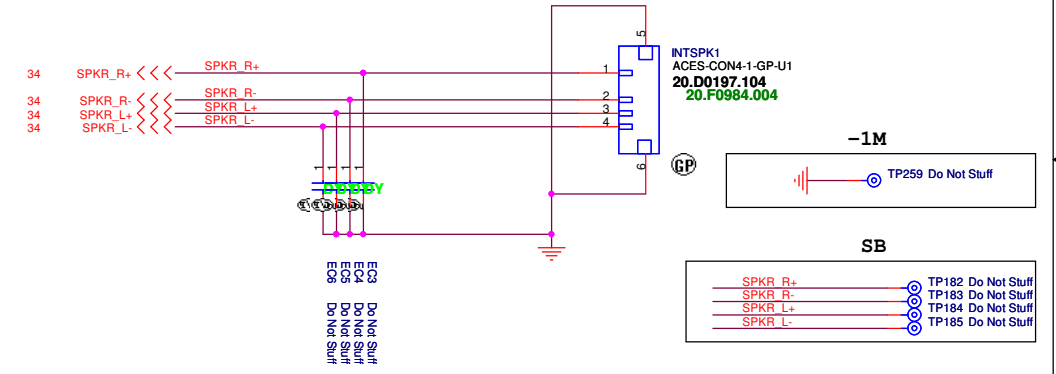


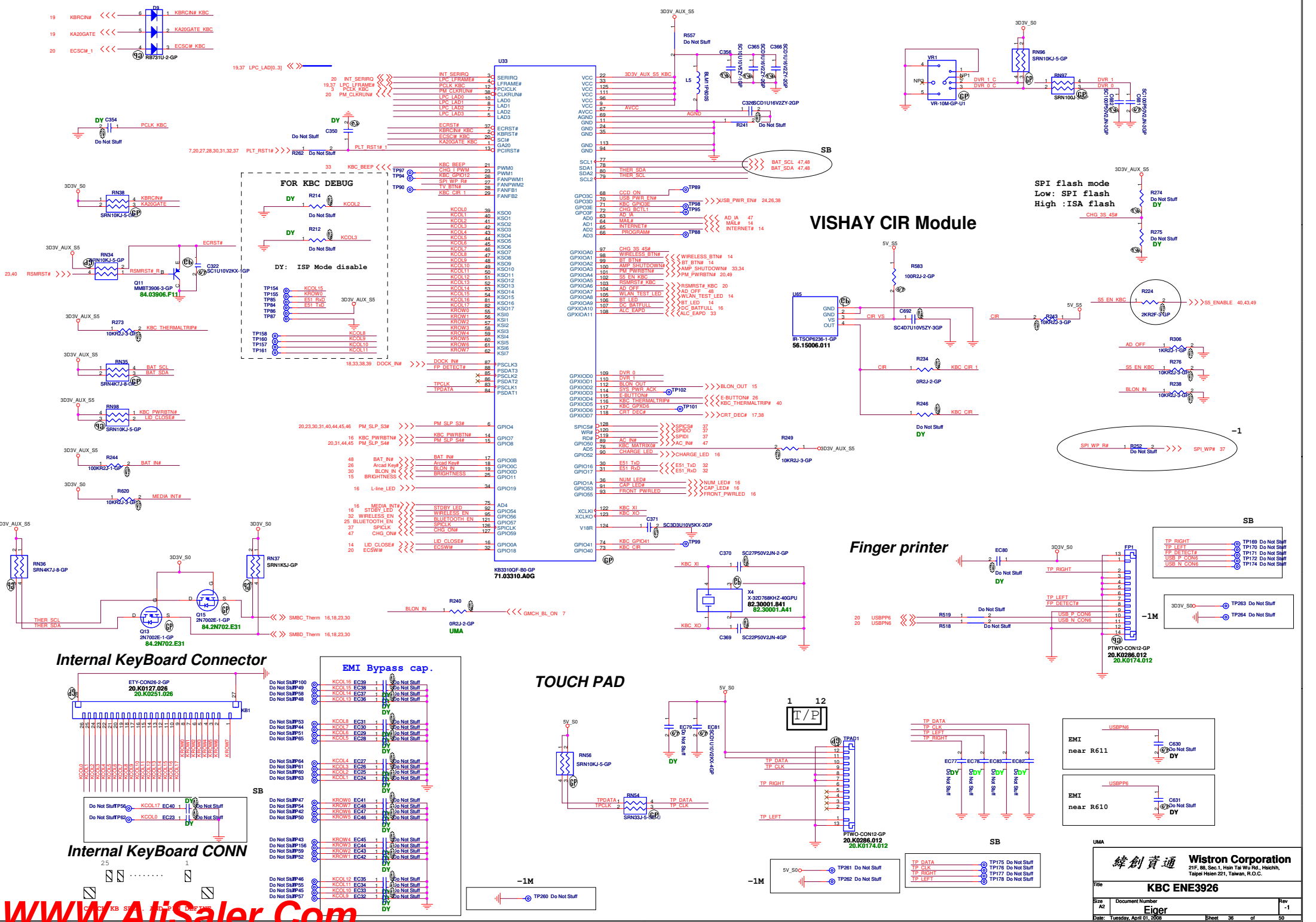
SUBWOOFER CONN.

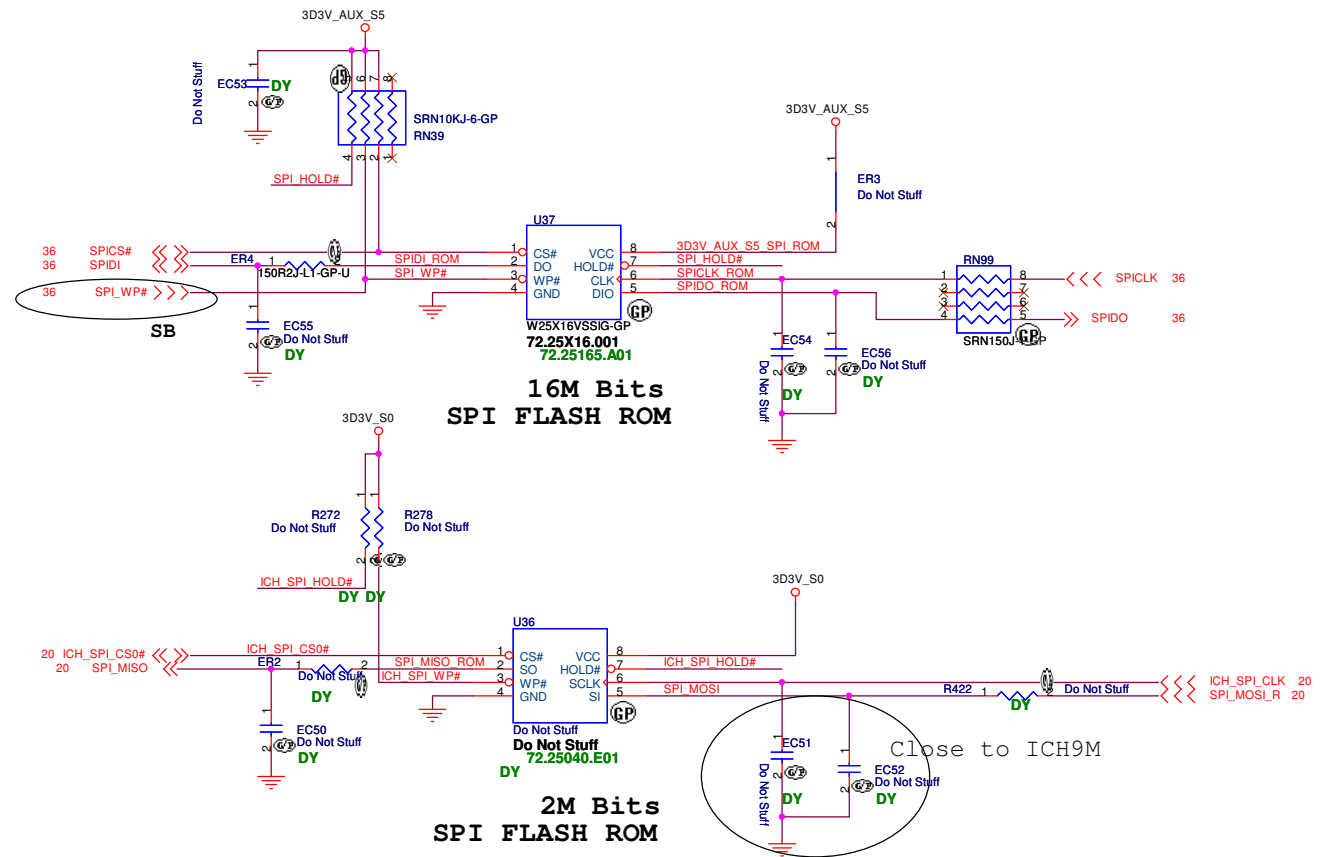




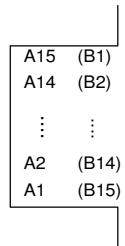
Internal Speaker





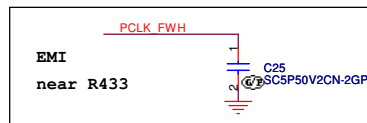
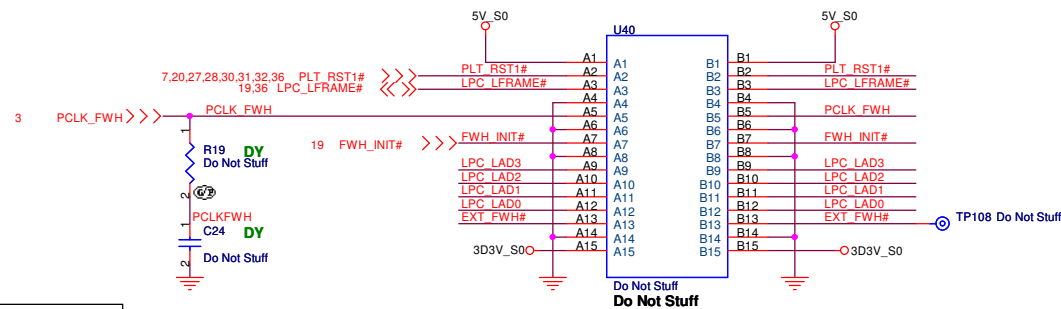


TOP VIEW



(BOTTOM VIEW)

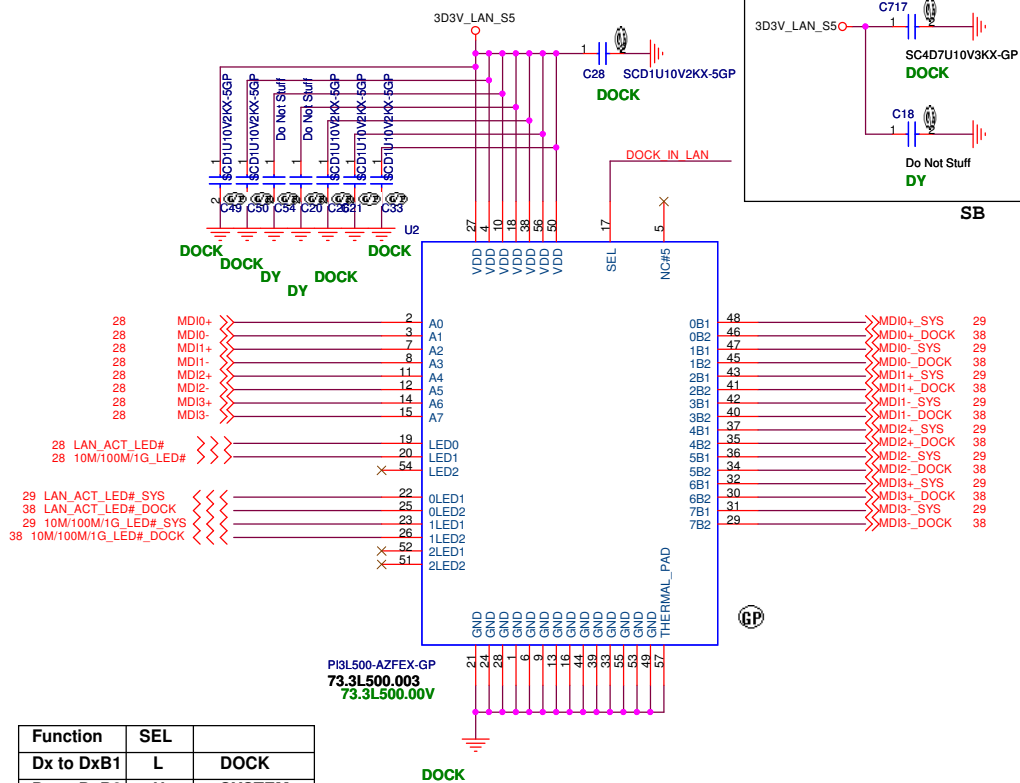
GOLDEN FINGER FOR DEBUG BOARD



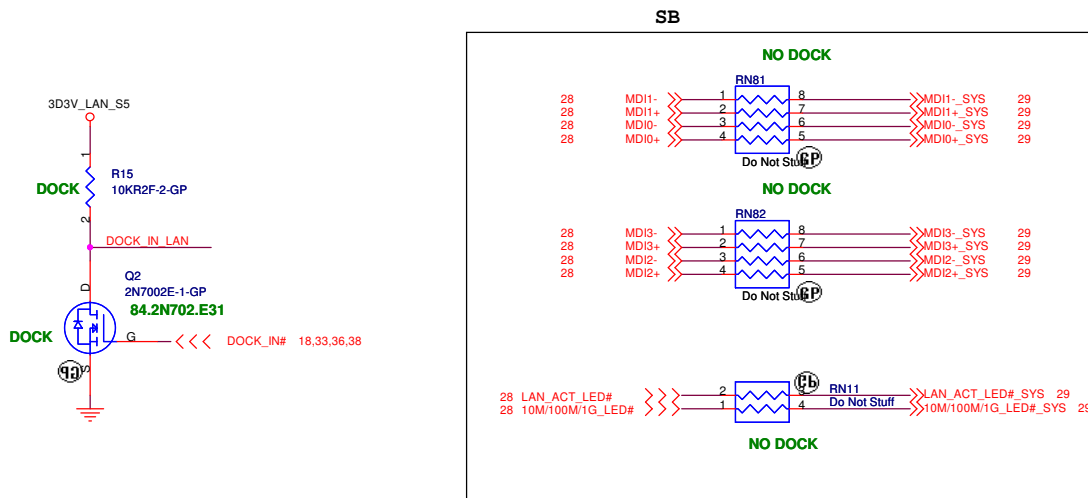
UMA

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LAN switch

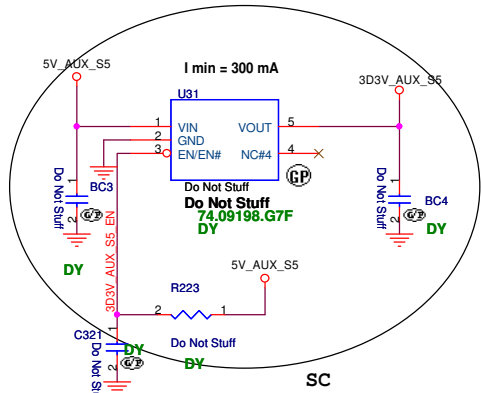


Function	SEL	
Dx to Dx B1	L	DOCK
Dx to Dx B2	H	SYSTEM

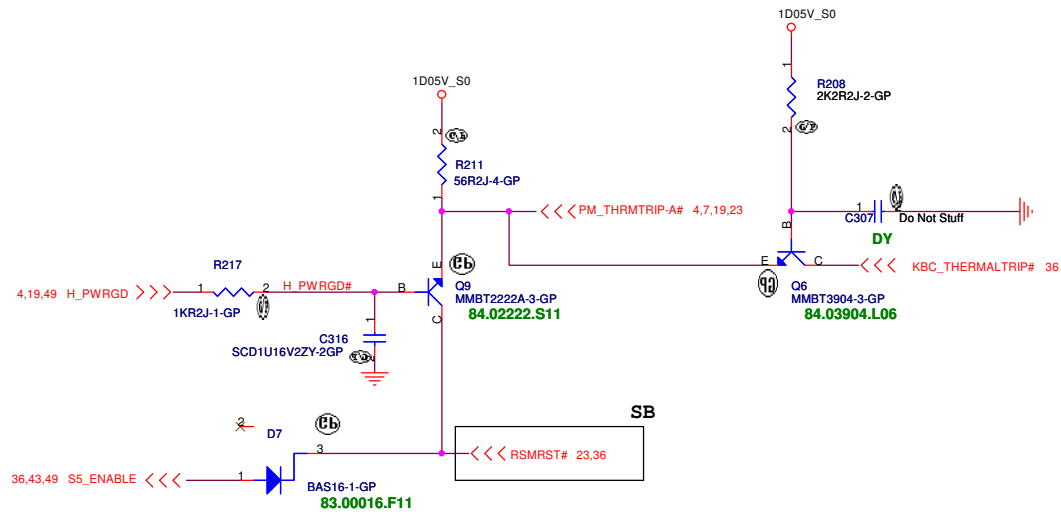
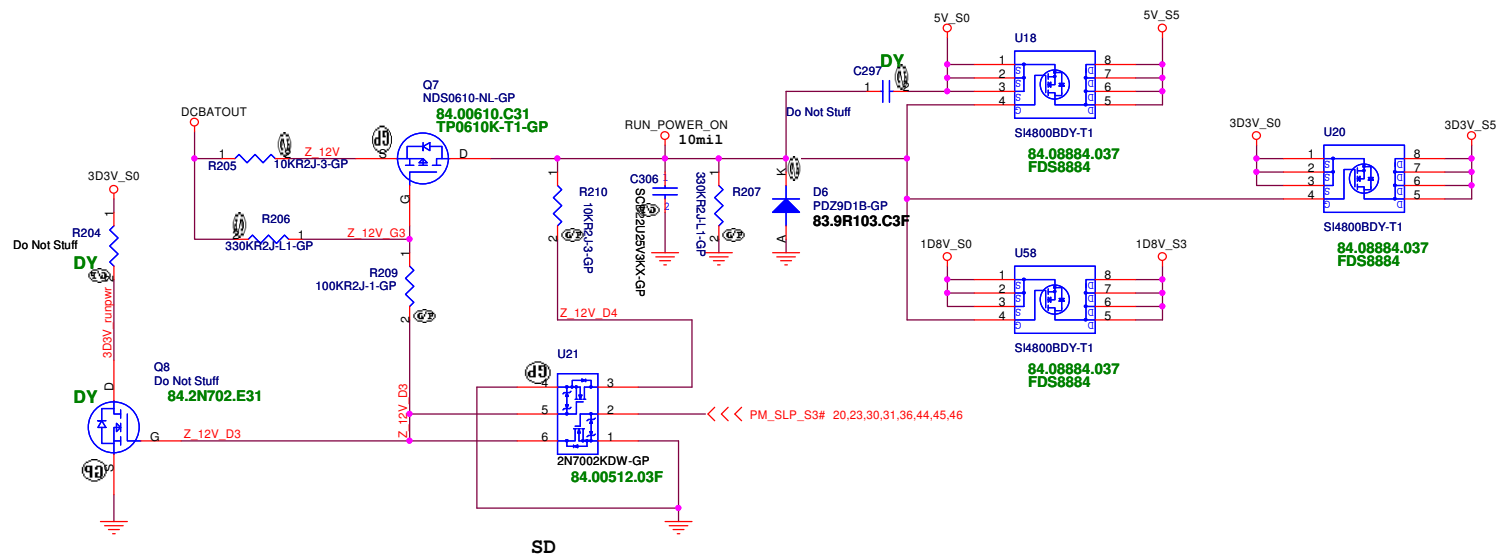


Aux Power

3D3V_AUX_S5



Run Power



UMA

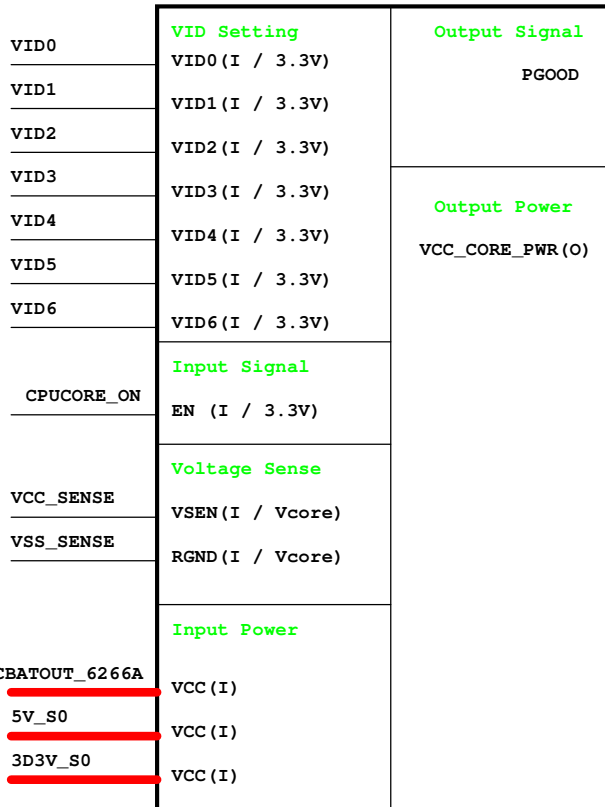
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Taipei Hsien 221, Taiwan, R.O.C.

Title	<i>RUN POWER and 3D3V_AUX_S5</i>
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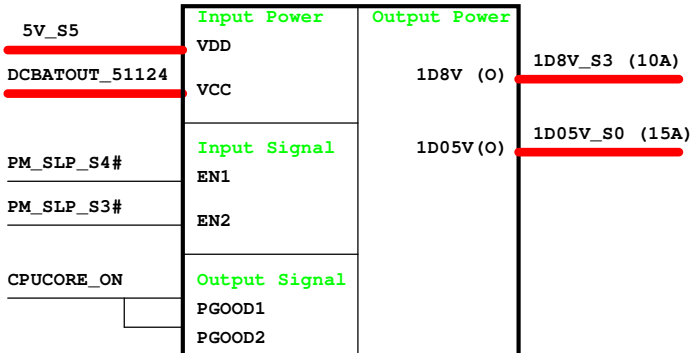
Size	Document Number	Rev
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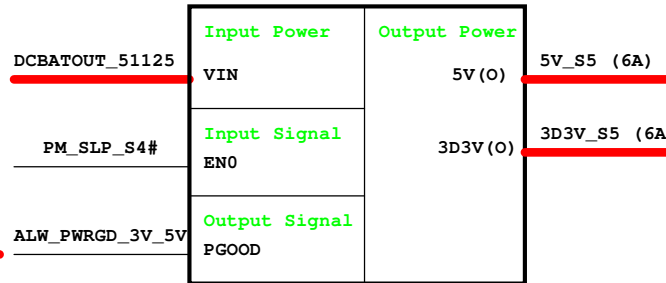
CPU_CORE
ISL6266A



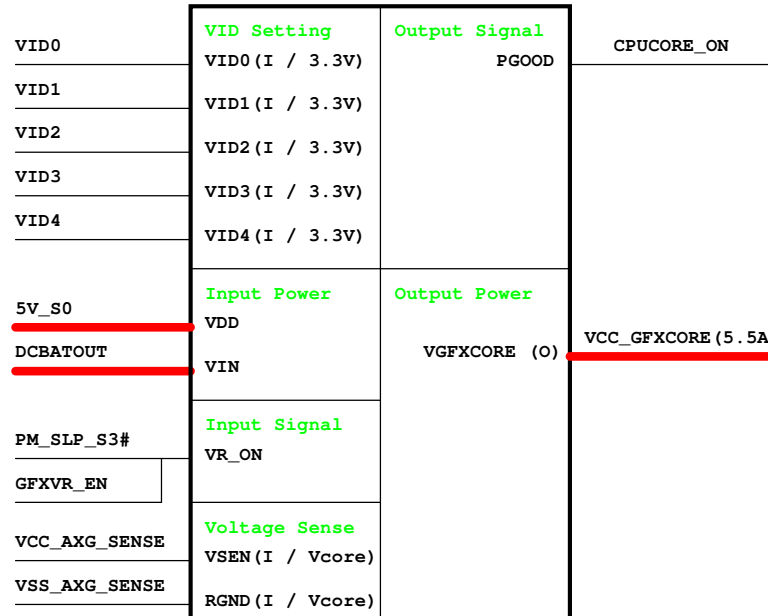
TPS51124
1D8V/1D05V



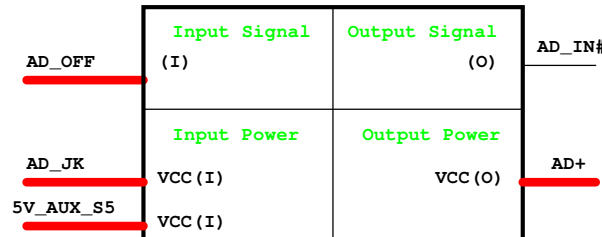
TPS51125
5V/3D3V



GFX_CORE
ISL6263A



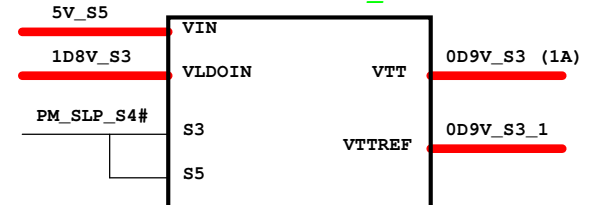
Adapter



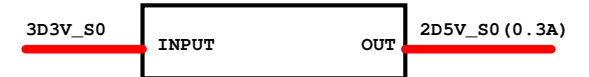
RT9018A
1D5V_S0



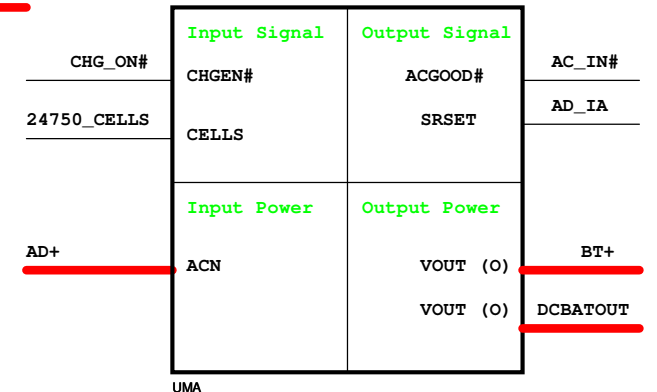
RT9026 0D9V_S0



G9131 2D5V_S0



Charger BQ24750



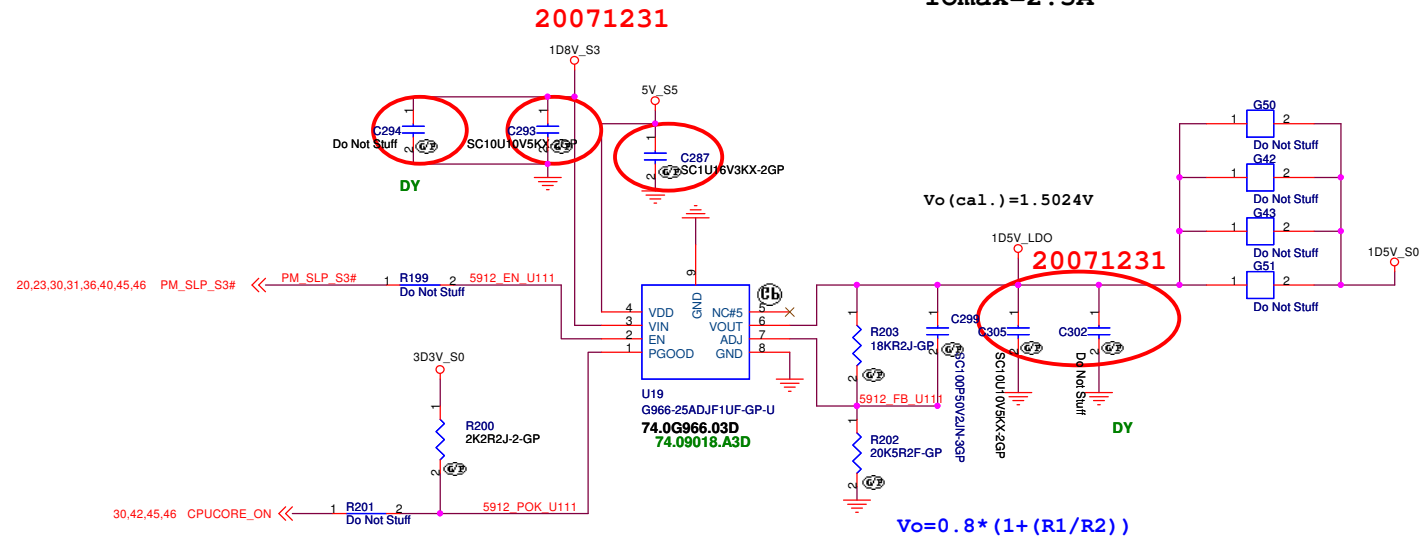
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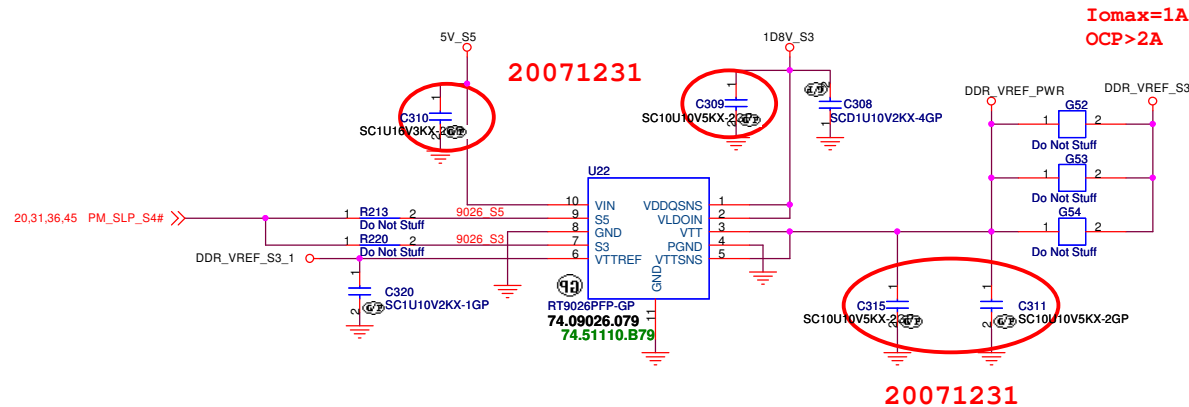
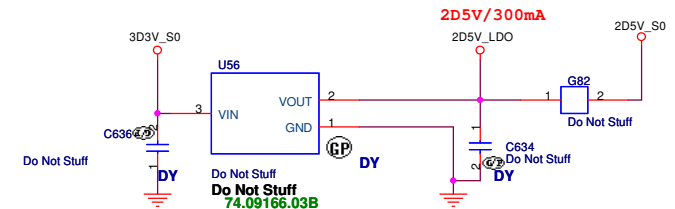
Title			Power Sequence Logic	
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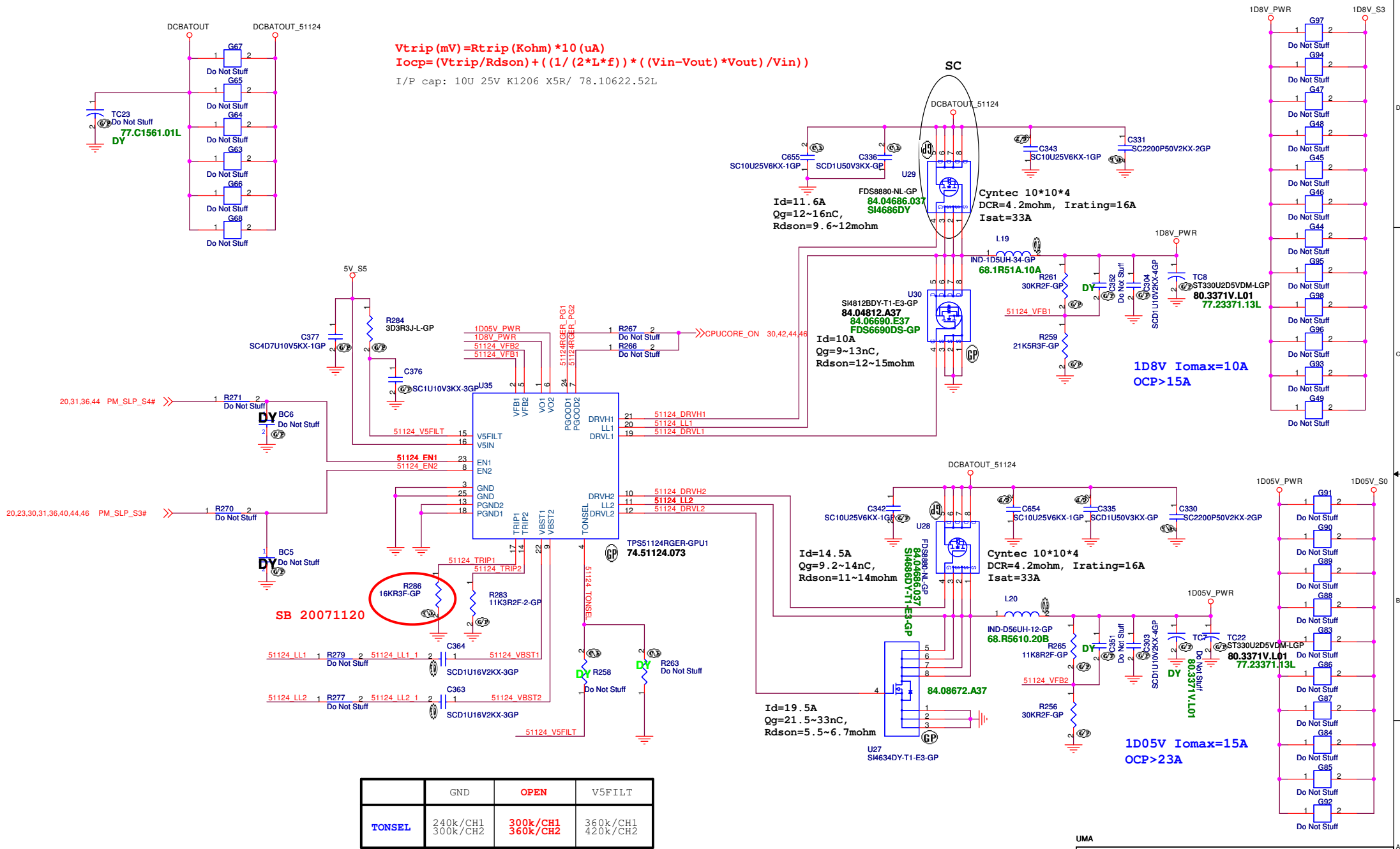


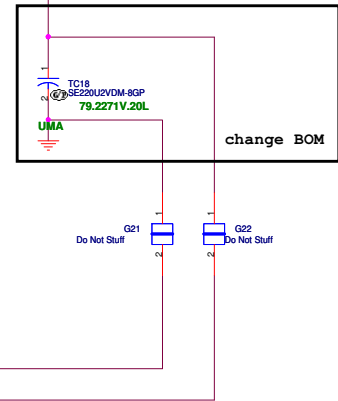
1D5V_S0
Iomax=2.5A

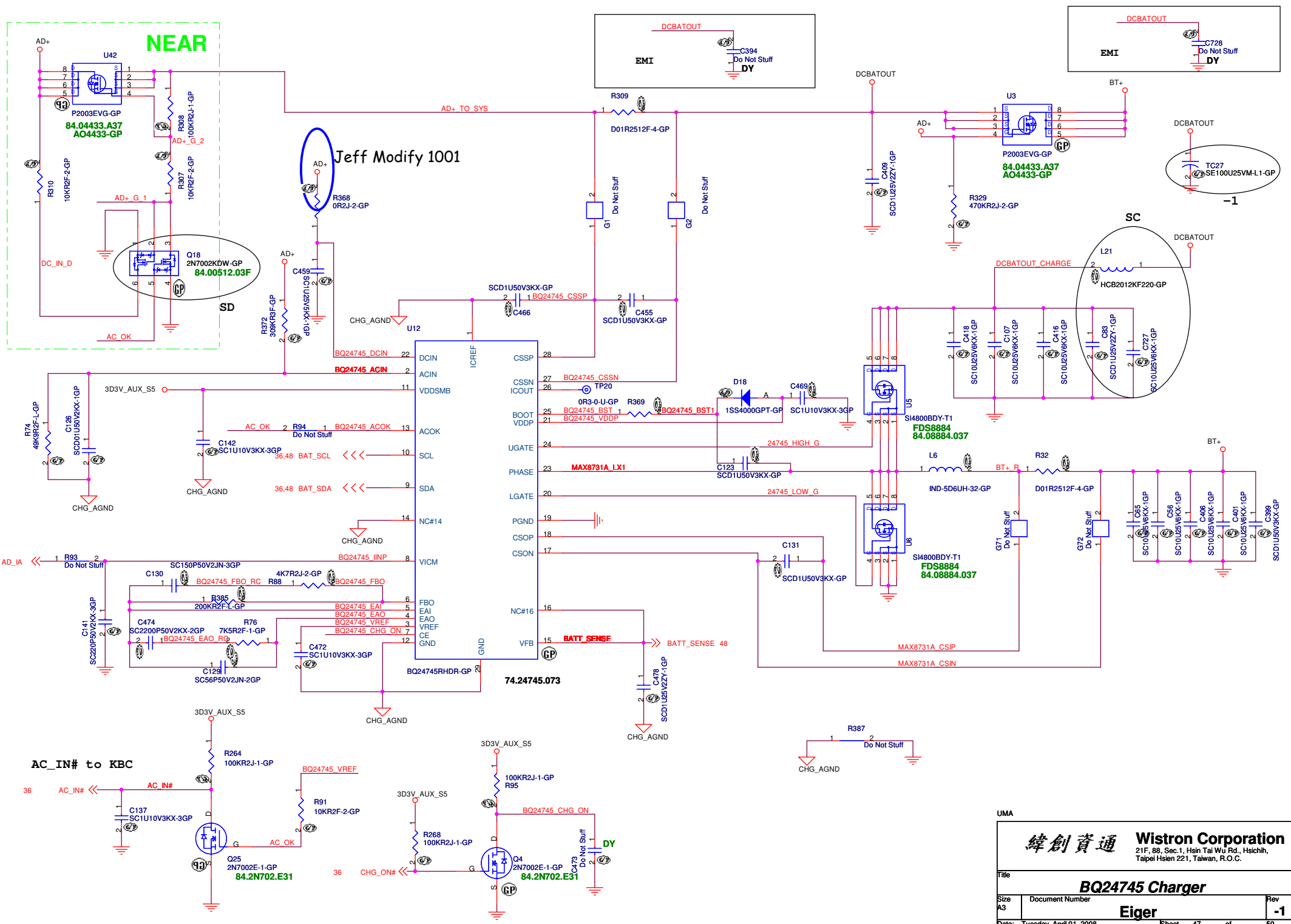


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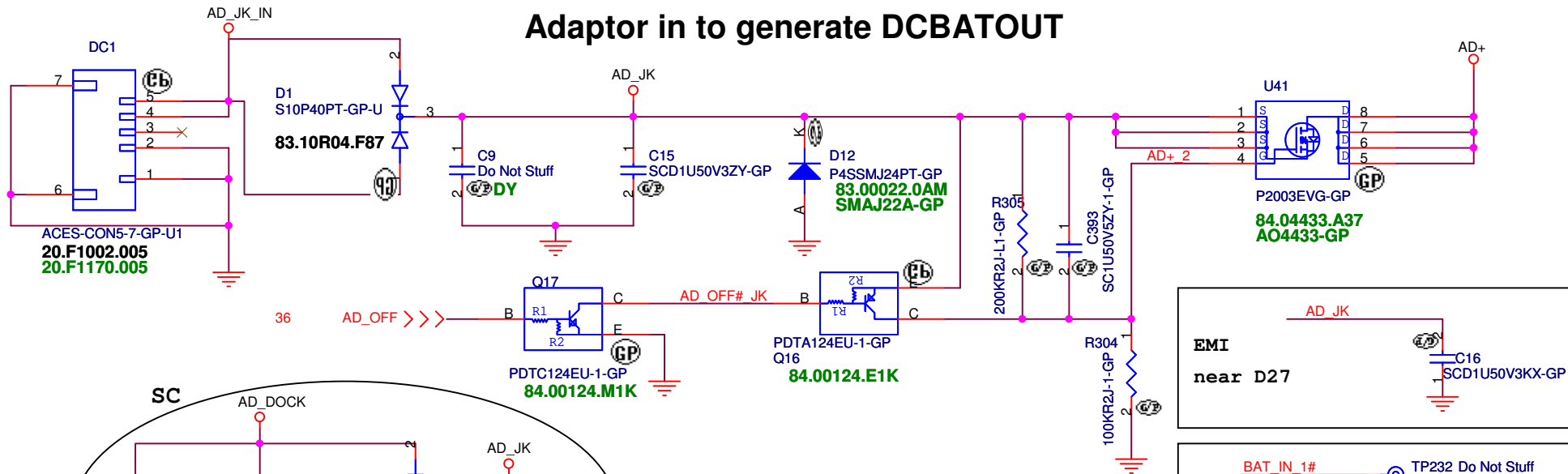




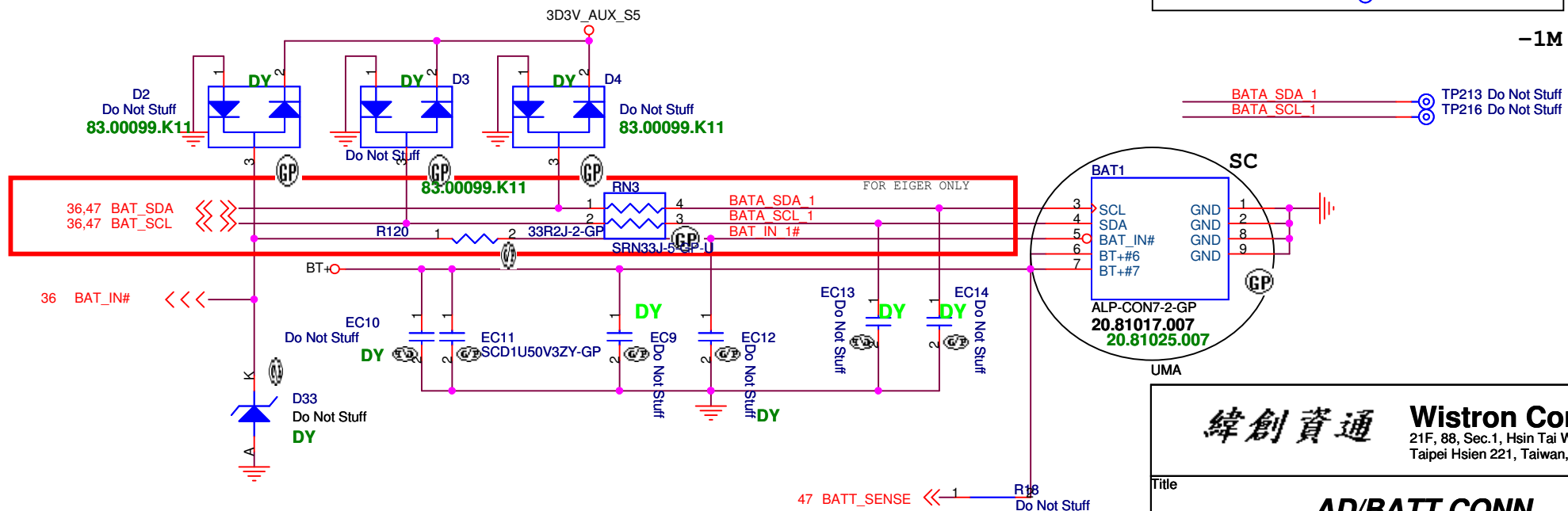




Adaptor in to generate DCBATOUT

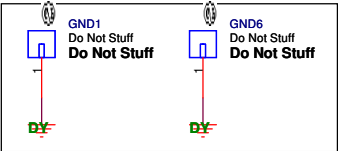
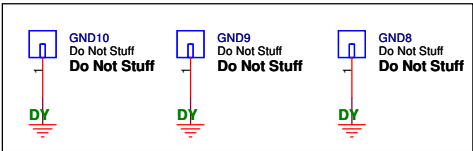
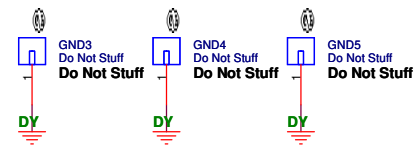


BATTERY CONNECTOR

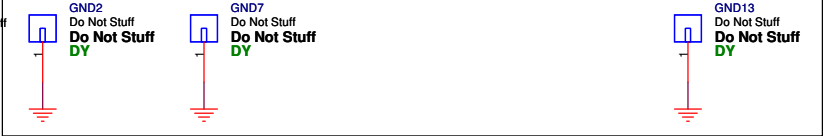
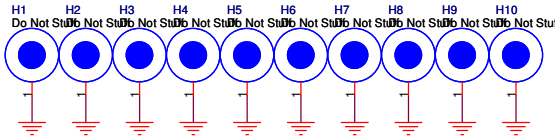


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Taipei Hsien 221, Taiwan, R.O.C.

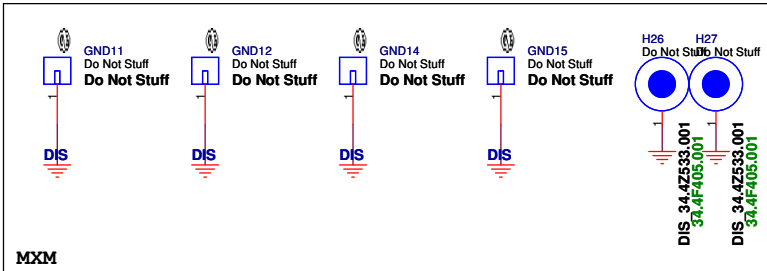
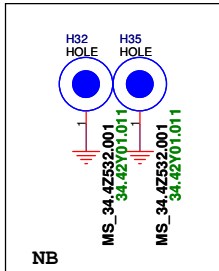
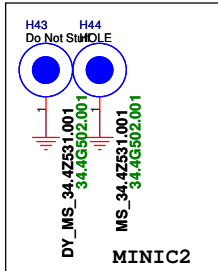
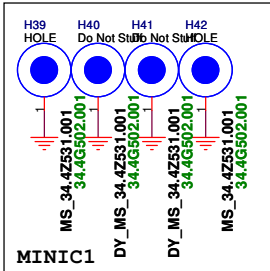
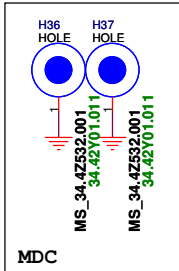
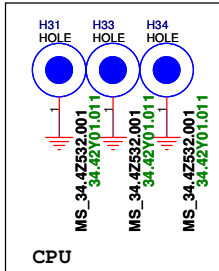
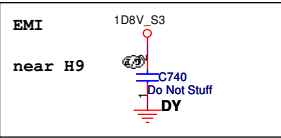
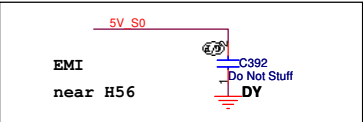
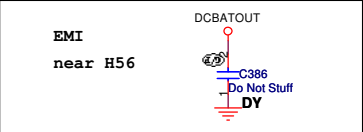
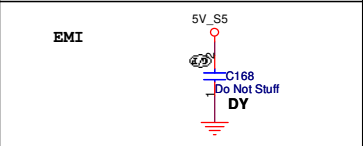
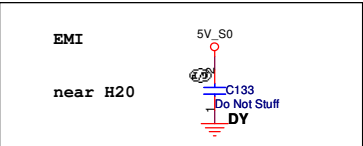
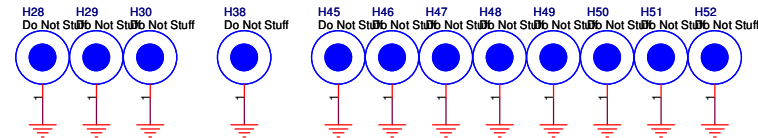
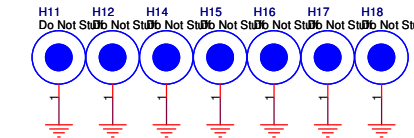
Title			AD/BATT CONN	
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			-1	
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SB



HDD



SB

Check test point

- 3D3V_S0 TP92 Do Not Stuff
- 3D3V_AUX_S0 TP223 Do Not Stuff
- 3D3V_S0 TP173 Do Not Stuff
- 5V_S0 TP224 Do Not Stuff
- 20,36 PM_PWRBTN# TP222 Do Not Stuff
- 4,19,40 H_PWRGD TP221 Do Not Stuff
- 36,40,43 S5_ENABLE TP166 Do Not Stuff
- 4,6 H_CPURST# TP133 Do Not Stuff

Test Point放在Dimm Door打開可量測處

UMA

Eiger Schematic EC Tracking Record LAB Dec.10 , 2007
EC #/ Page / Description / Part Affected

- EC SB01/07/ DY R175 (fix can not boot)
- EC SB02/07/ change R184 (intel spec change)
- EC SB03/10/ mount L2,C221 (intel spec change)
- EC SB04/15/ modify LCD2 pin define(add dig-MIC,backlight)
- EC SB05/17/ DOCK_IN_CRT# logic change
- EC SB06/18/ change HDMI level shift IC setting
- EC SB07/19/ change R606(meet HDA SPEC)
- EC SB08/23/ change PURE_HW_SHUTDOWN# ,PM_THRMTRIP-A# schematic
- EC SB09/26/ change C648 ,deltree poly switch
- EC SB10/27/ change R555,R557,R559 (vendor request)
- EC SB11/30/ change R612 (vendor request)
- EC SB12/34/ add C711 (fix audio noise)
- EC SB13/36/ add SPL_WP# (BIOS wirte protect)
- EC SB14/38/ add CRT_DEC# (Acer change spec)
- EC SB15/38/ add dock/no dock option schematic
- EC SB16/40/ D7(power sequencing)
- EC SC01/16/ R595,R596,R597,R598(LED)
- EC SC02/18/ HEMI level shift & switch solution change
- EC SC03/19/ ESATA function
- EC SC04/23/ H/W Thermal shut down,power off Sequence
- EC SC05/24/ Add ESATA circuit
- EC SC06/30/ Add R116(MXM aczrst# Acer request)
- EC SC07/33/ Add audio gound
- EC SC08/34/ Change audio AMP circuit
- EC SC09/38/ Add RC circuit to reduce audio noise
- EC SC10/40/ 3D3V_AUX_S5 from U32 internal LDO
- EC SC11/43/ Change 5V to 5.1V
- EC SC12/47/ Isolate Change IC switching high side MOS input power
- EC SC13/48/ Isolate AD19V in and Dock19V in

UMA			
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
EC Tracking Record			
Size	Document Number		Rev
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Date:	Tuesday, April 01, 2008		Sheet 50 of 50